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MANUFACTURING METHODS AND TECHNOLOGY ENGINEERING FOR TAPE CHIP --ETC(U)  
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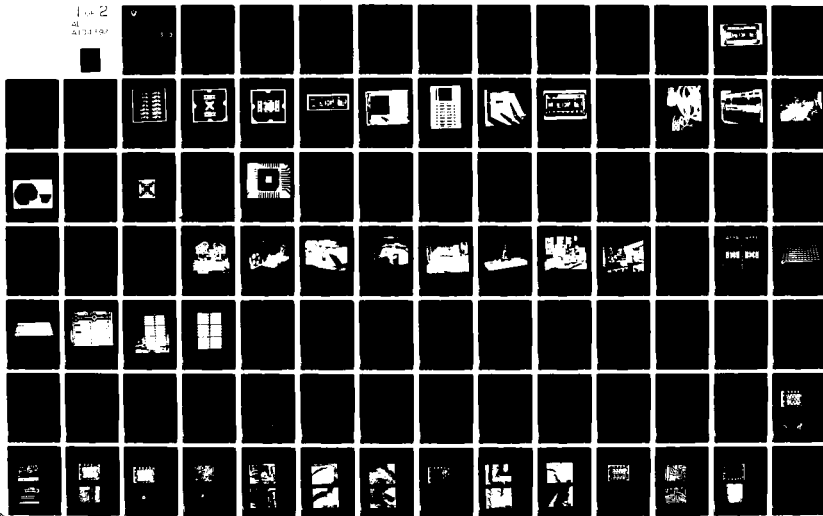
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Research and Development Technical Report  
DELET-TR-77-0526-F

**MANUFACTURING METHODS AND TECHNOLOGY  
FOR TAPE CHIP CARRIER**

William R. Rodrigues de Miranda  
Wilford O. Perry  
Paul H. Shreve  
Honeywell Inc.  
Clearwater, Florida 33516

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August 1981

Final Report for Period 30 June 1977 to 31 August 1981

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Electronics Technology and Devices Laboratory

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number) This contract was aimed at establishing the feasibility of an assembly line for manufacturing hybrid microcircuits using tape automated bonding (TAB). This report describes work performed during the pilot line phase of the contract. A purpose of the MM&T work was to demonstrate the viability of the manufacturing approaches with TAB and		

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the determination of the associated yield and cost factors. This report includes an overview of these factors, the methods and equipment employed in the manufacture of approximately 1200 hybrid microcircuits with TAB, and the qualification test results of the circuits using the TAB mounted devices.

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## Section 1

### INTRODUCTION

Tape Automated Bonding\* (TAB) applications for military hybrid microcircuits have seen nearly five years of development. In the first several years, material combinations, bump and tape configurations and bonding techniques were explored under R&D contracts. Small to moderate quantities of different configurations were built and tested successfully. More recently emphasis was placed on the demonstration of production feasibility through Manufacturing Methods and Technology (MM&T) contracts.

The purpose of the MM&T work is to demonstrate the viability of the manufacturing approaches with TAB and the determination of the associated cost and yield factors. The established TAB manufacturing techniques included mounting of semiconductor chips on reels of sprocketed film or tape, burn-in and testing of these chips on tape and their placement on the hybrid substrates. The Army is interested in utilizing TAB technology for the manufacture of hybrid microcircuits for military electronic applications when advantageous for economic reasons or desirable from the viewpoint of increased reliability.

TAB technology can be implemented with a number of different materials and bonding technologies as described in the final reports of the R&D work\*\*. At the start of the MM&T phase, specific selections of available materials and techniques were made, keeping in mind the requirements for performance and reliability. The process begins with a wafer in which all devices have gone through all the normally required semiconductor processing. The wafer is then given a protective cover of silicon nitride prior to the bumping process in order to more precisely define the bump geometry on the pads of each device and to offer greater protection of the chip surface. Barrier layer metallization of the pads on the semiconductor wafer consists of titanium, palladium and gold. The bump itself is plated of pure gold. The lead frame is electro-deposited copper, plated with 100 microinches of gold. The leads are thermocompression bonded to the bumps resulting in gold/gold bonds. The alumina substrates have been screen printed with mixed bonded gold paste. The outer lead bonds were thermocompression bonded, again resulting in gold/gold metallurgy. The chip is attached to a screened gold pad on the substrate with silver filled epoxy.

---

\*Also referred to as TCC (Tape Chip Carrier) and TCLF (Tape Carrier Lead Frame)

\*\*Reports ECOM-76-1401F, September 1977 and DELET-TR-2708F, September 1979 both entitled "Tape Chip Carrier for Hybrid Microcircuits".



This report is compiled as an overview of the methods and equipment employed in the successful manufacture of approximately 1,200 hybrid microcircuits with TAB technology. The manufacturing cycle included processing more than 10,000 chips, manufacture and plating of 7,500 lead frames, inner lead bonding and testing of more than 6,000 chips on tape, and outer lead bonding of nearly 5,000 chips.

## Section 2

### THE HYBRID MICROCIRCUIT

The hybrid is an 8 bit synchronous counter shift register consisting of two 54LS161A synchronous 4 bit counter chips, one 54LS165 parallel load 8 bit shift register chip and one capacitor chip. The hybrid will be referred to hereafter as the "E/M Sync Counter" or "SYNC Counter".

It is designed such that it is operational at its intended frequency of 18 MHz. Any or all 8 bit word patterns may be realized in the Sync Counter. Integrity of any 8 bit word is maintained in parallel load/transfer to the shift register. The 8 bit word, loaded in parallel, is shifted out of the register with the control gated serial clock. Serial data may be loaded into and out of the register with the control gated serial clock.

This hybrid is part of an Electrically Suspended Gyro (ESG) navigation system, currently being built in a quantity of several hundred systems, including the B-52 Navigation System, the Precision Navigation System (PNG) and one or more classified programs. A circuit schematic is shown in Figure 2-1. A photograph of the completed device is shown in Figure 2-2.

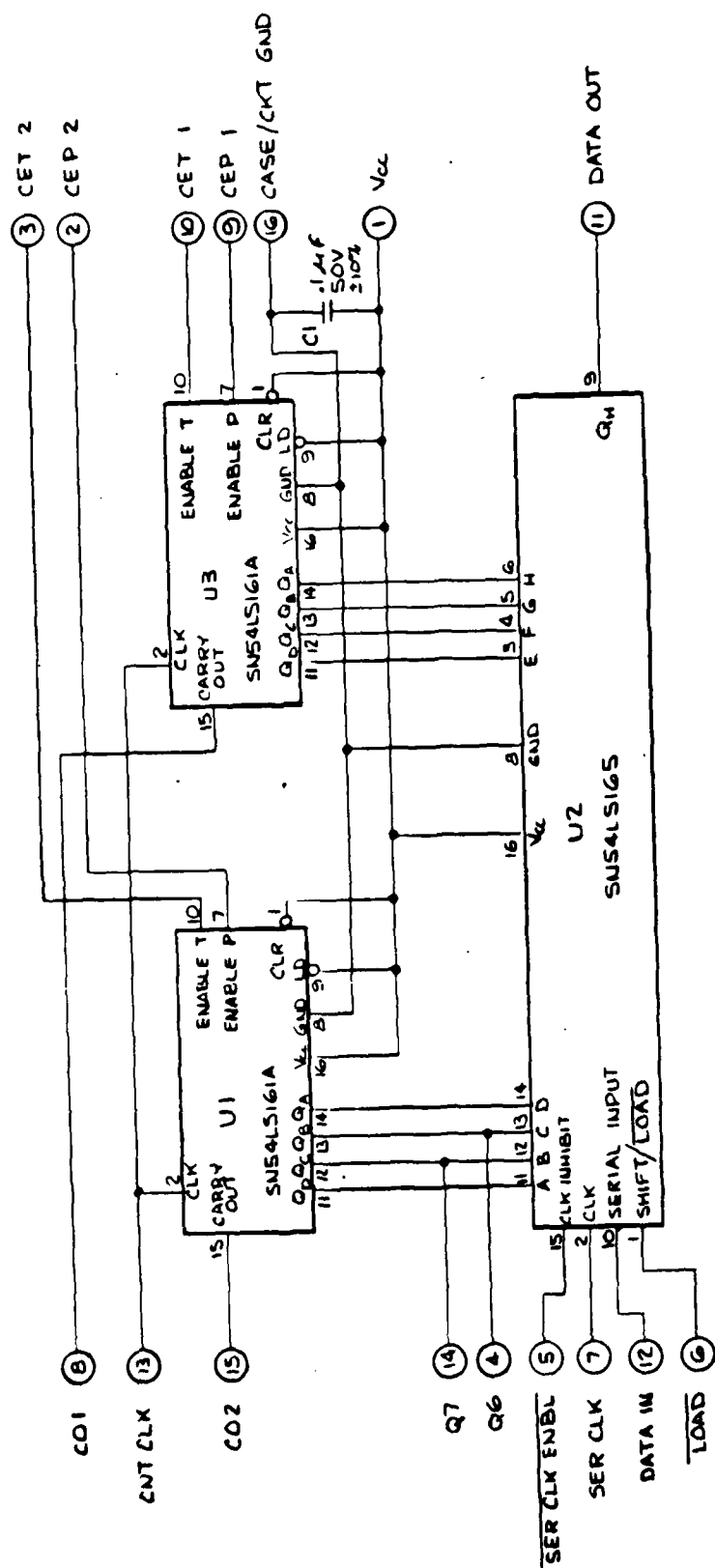
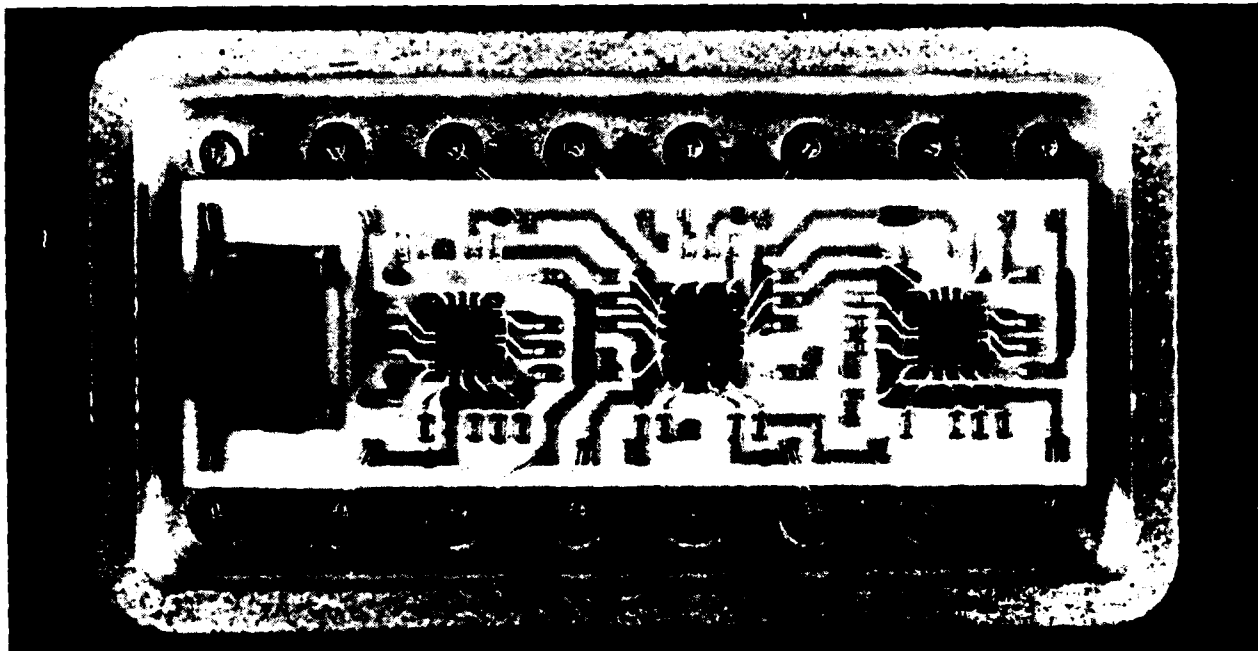


Figure 2-1. E/M Sync Counter Schematic



*Figure 2-2. E/M Sync Counter After Assembly*

### Section 3

#### THE ASSEMBLY SEQUENCE

Figure 3-1 shows schematically the assembly sequence as followed in the manufacture of the hybrids.

A substrate redesign/relayout took place as soon as basic circuit information became available. It was determined that the most economic screen printing configuration was a 14-up format on a 2x2 inch substrate (see Figure 3-2). The 2x2 substrates were prescribed by laser at P/M Industries in Portland Oregon, in order to allow breaking into individual substrates.

The semiconductor wafers were passivated with  $\text{Si}_3\text{N}_4$  at Honeywell's Colorado Springs facility, followed by barrier layer metallization at Honeywell SSEC in Plymouth, Minn. Bumping was done at Honeywell Avionics Division (AvD) in Florida, with established solid photoresist (Riston 211) lamination method.

Lead frame design and production of 1:1 art was done per established methods at AvD in Florida. Lead frames were manufactured by Honeywell's Phoenix facility (LISD). Plating was accomplished on our newly installed continuous plater in Florida at a rate of 1000 frames/hour. Inner lead bonding (ILB) was done on the Jade I-1000 automatic bonder, at a rate of 1000 per hour. Chips were handled on continuous reels of tape through inner lead bonding and testing.

Testing of chips on tape was to be accomplished with the new Automatic Test Handler which has been on order from the Jade Corporation but was not delivered in time for this program. The manual reel-to-reel tester was used, allowing only room temperature testing. Test rates of up to 400 chips per hour were achieved while interfaced with the Fairchild 5000 automatic tester.

After testing, the tape was cut into frames and mounted into 35mm slide carriers (see Figures 3-3 and 3-4), designed and patented by Honeywell. A quantity of devices was tested after burn-in on the working portion of the Automatic Test Handler, which was mounted on a temporary base. (See Figure 8-6).

In preparation of outer lead bonding (OLB) the 2x2 substrates were screen printed with epoxy for chip attach (see Figure 3-5).

Outer lead bonding (OLB) was accomplished on the Jade 4810 machine at a rate of about 60 chips per hour. Initially the 2x2 substrate (14-up configuration) was mounted in the substrate holder and populated, placing rows of 161A and 165 chips (see Figure 3-6). After a problem with substrate cracking caused unacceptable losses, the 2x2 substrate was broken into individual substrates (Figure 3-7) which were bonded one at a time in a special holder (see Figure 3-8). The rate for this operation dropped to about 40 chips per hour. The approach to use a 14-up configuration on a 2x2 substrate can be used in future projects if precautions are taken with regard to substrate flatness and proper seating in the holder. Minor modification in the holder may be required. Trial bonds of the prelaser scribed substrates were performed without difficulty during test set-up. However, frequency/rep. rate of laser and/or power output of the laser to work surface was altered by the vendor causing heat build up and microcracking of substrates actually used in this work resulting in difficulties observed. It is not anticipated that properly scribed substrates would result in further difficulties of this nature.

After OLB the populated substrate was mounted in the header, the capacitor was added, followed by pin-out bonding with conventional thermosonic bonding techniques. The completed TAB Sync Counter is shown in Figure 2-2. As comparison, a wire bonded (conventional) Sync Counter is shown in Figure 3-9.

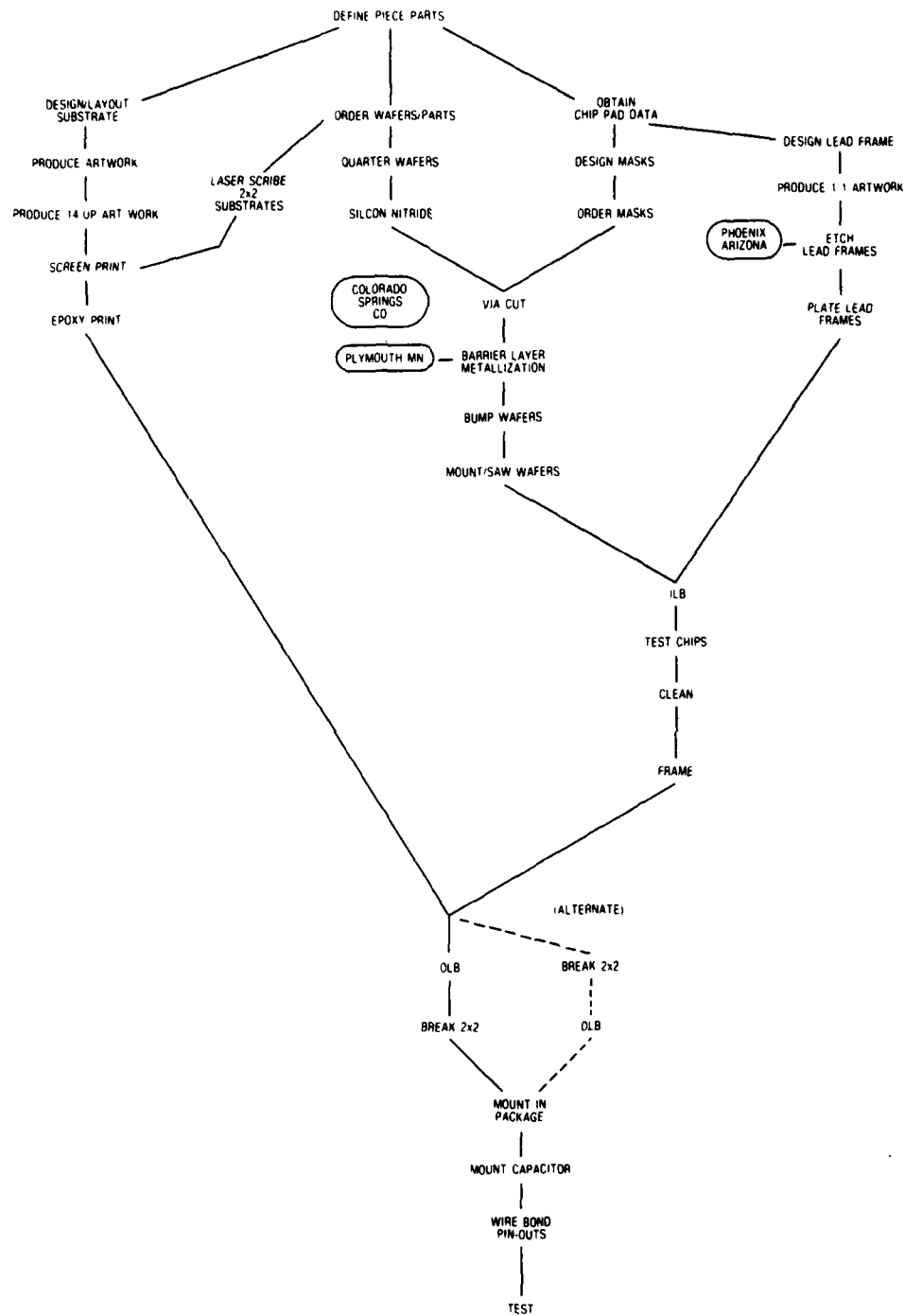
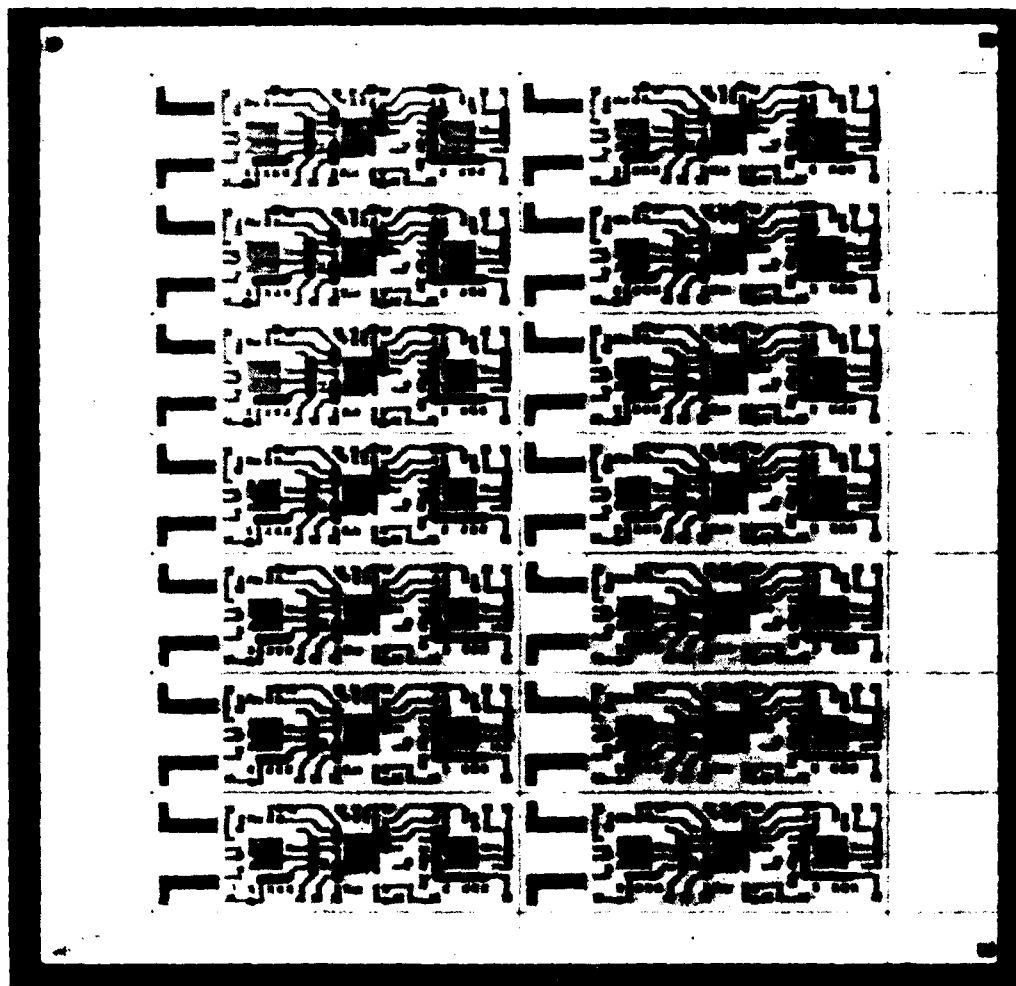
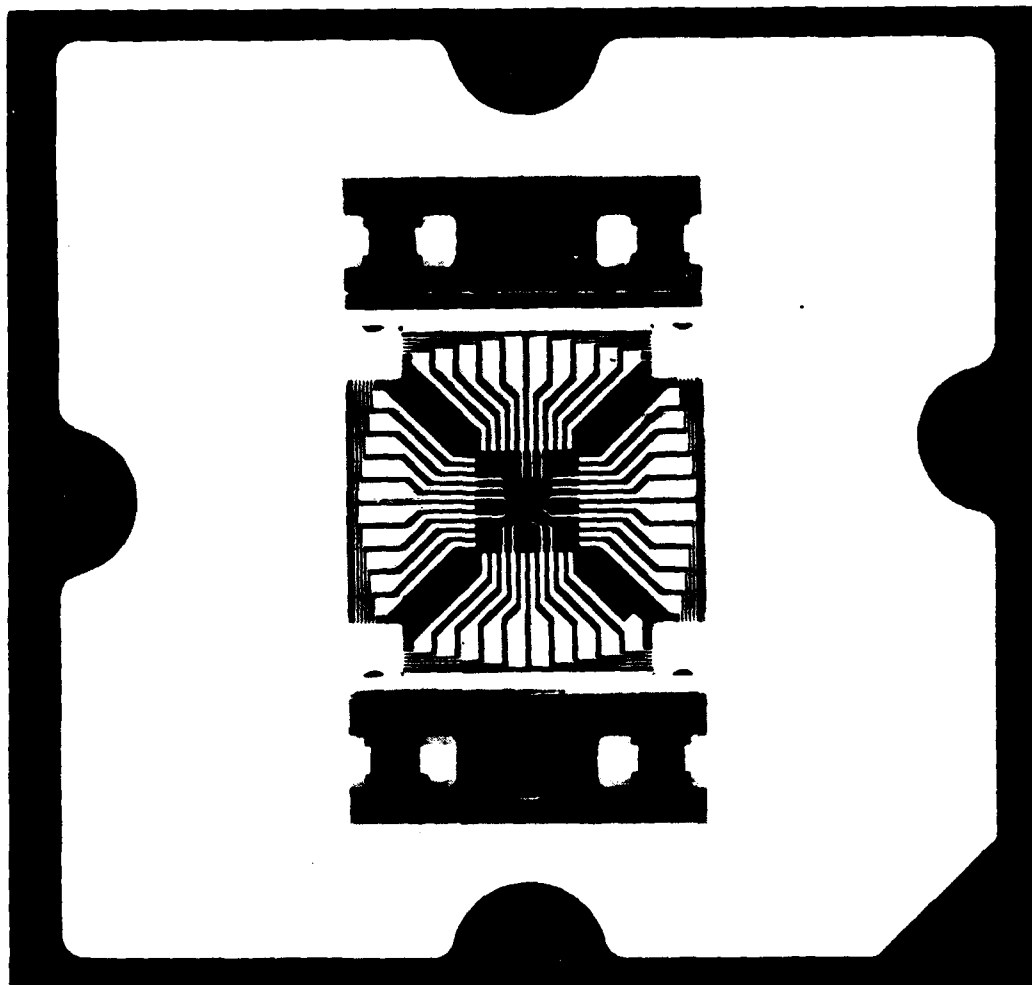


Figure 3-1. Assembly Sequence of E/M Sync Counter

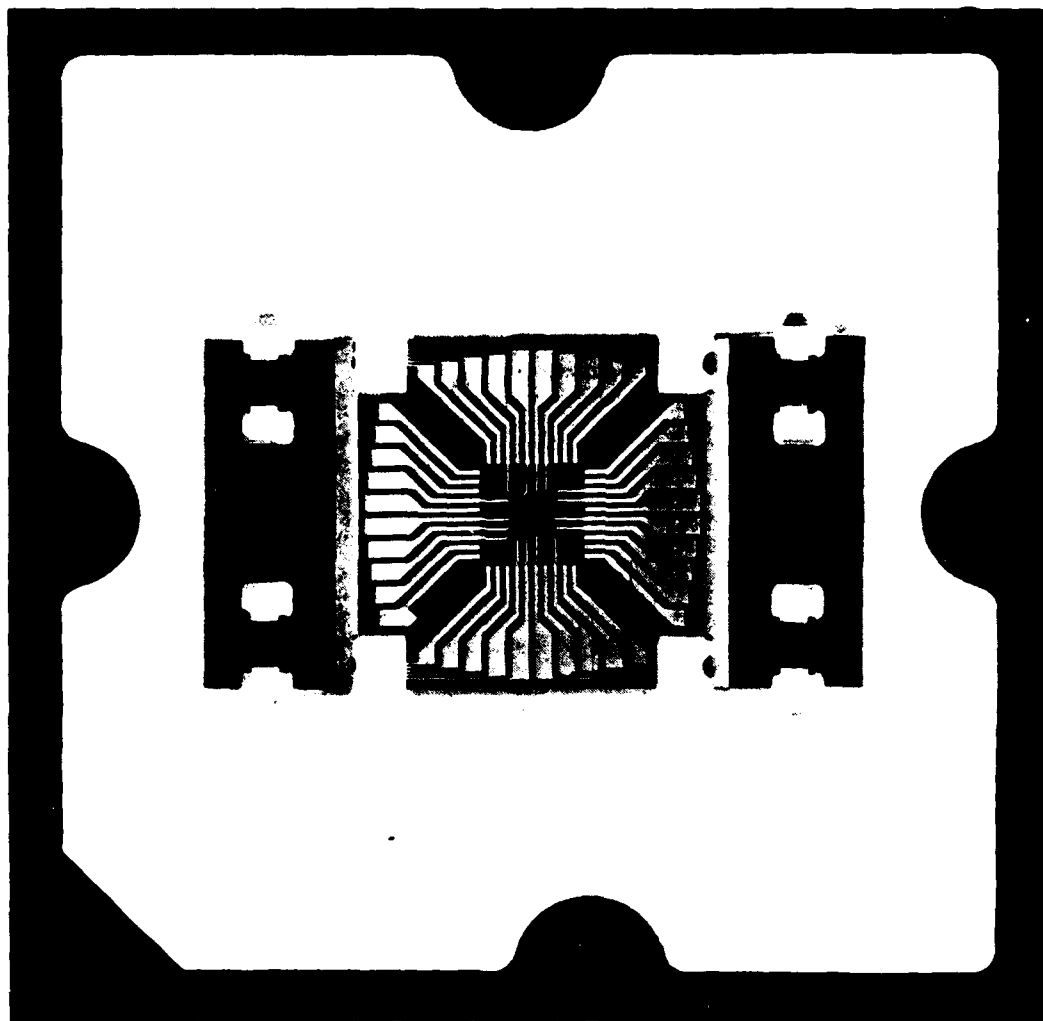


*Figure 3-2. E/M Sync Counter as Screened - 14 Up*

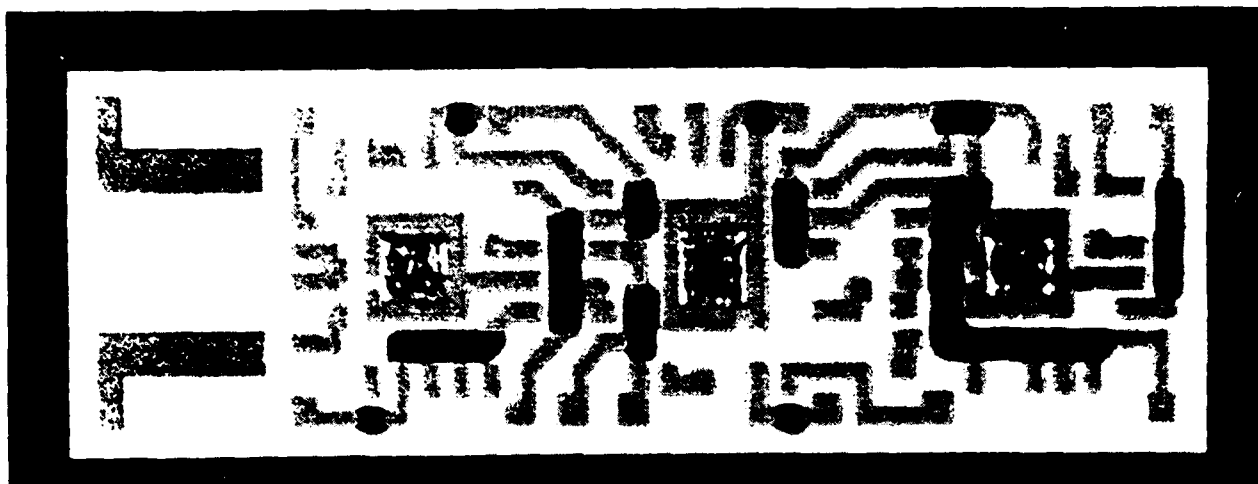




*Figure 3-3. 54LS161A on Slide Carrier.*



*Figure 3-4. 54LS165 on Slide Carrier*



*Figure 3-5. E/M Sync Counter After Epoxy Screen*

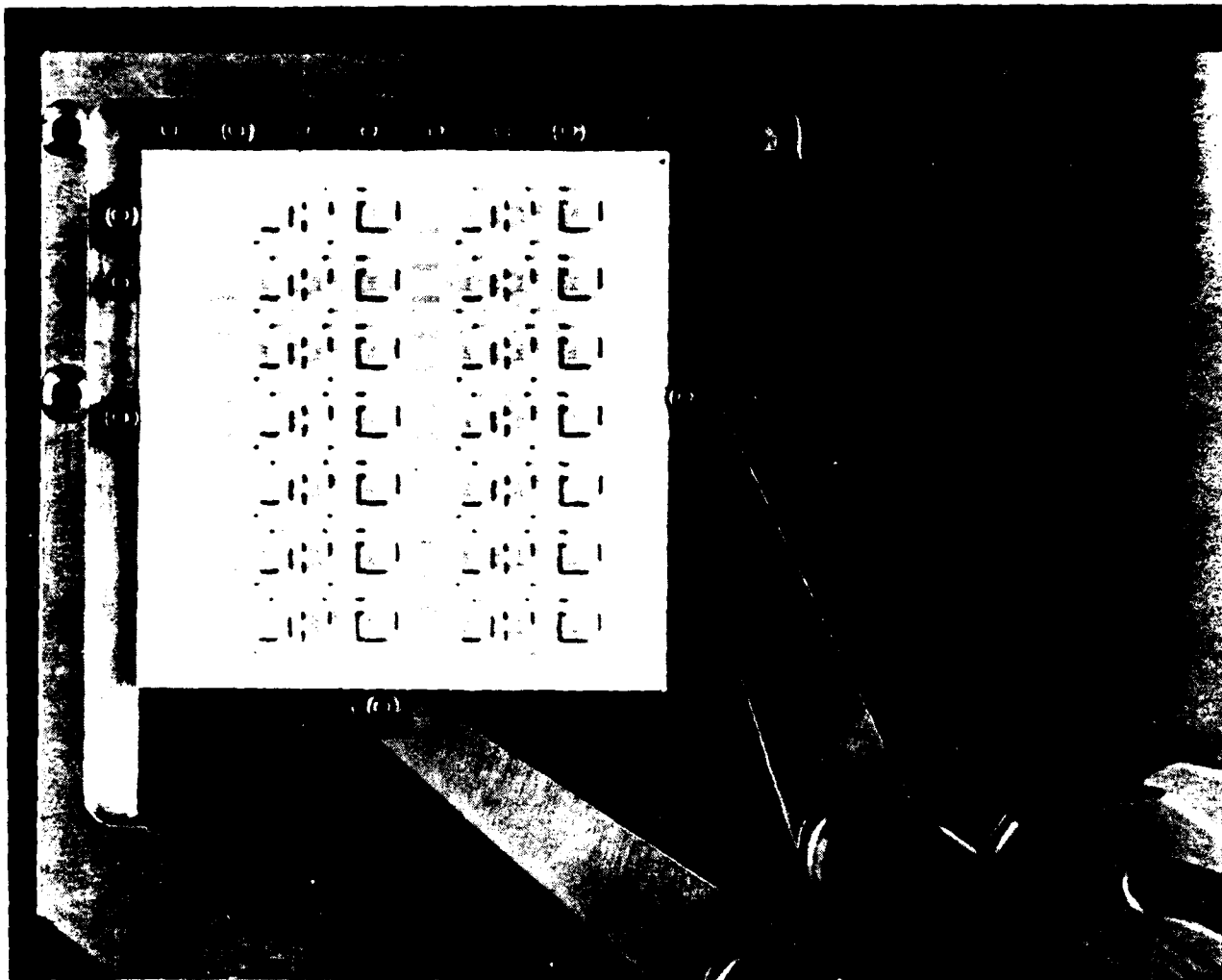


Figure 3-6. 2x2 Substrate in OLB Holder

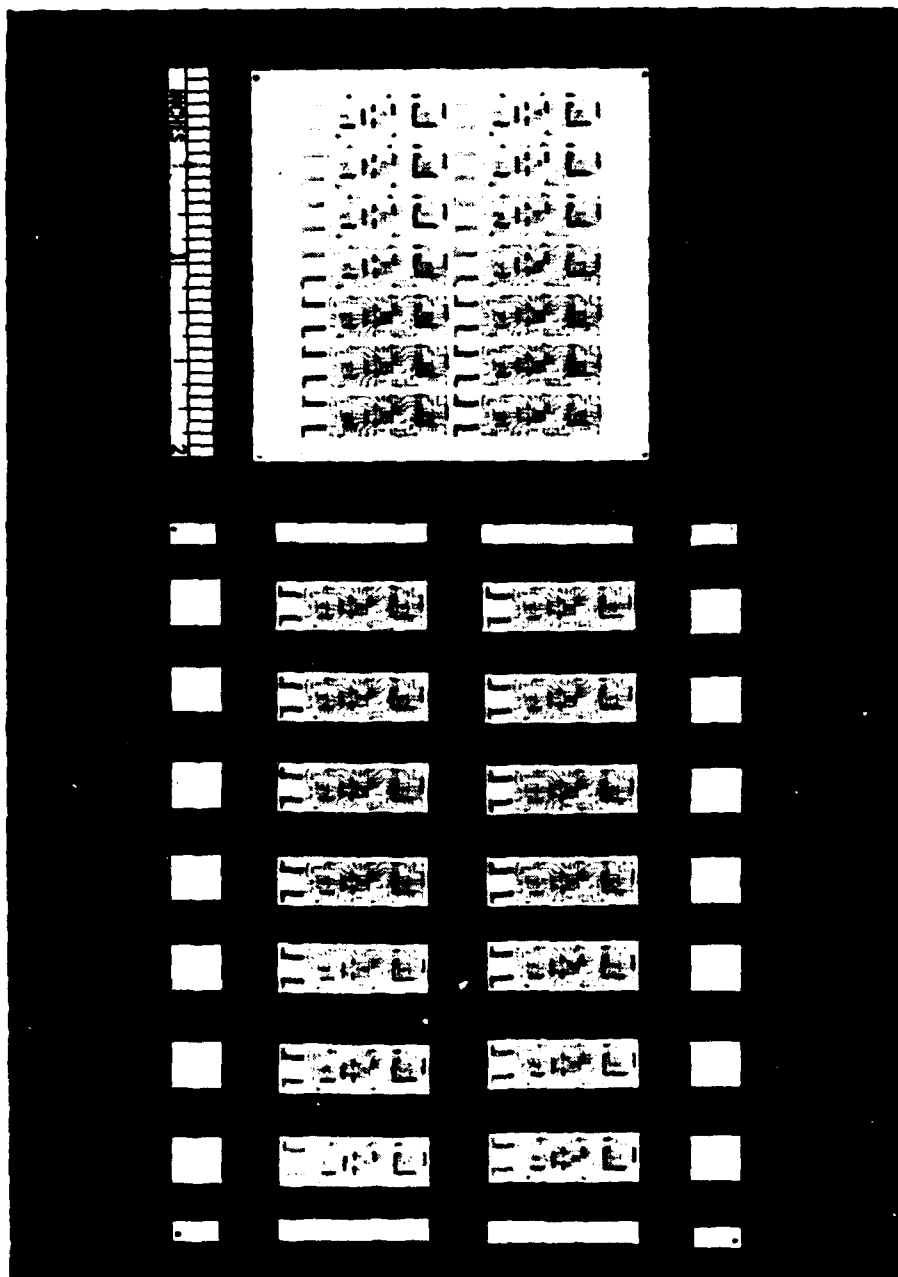
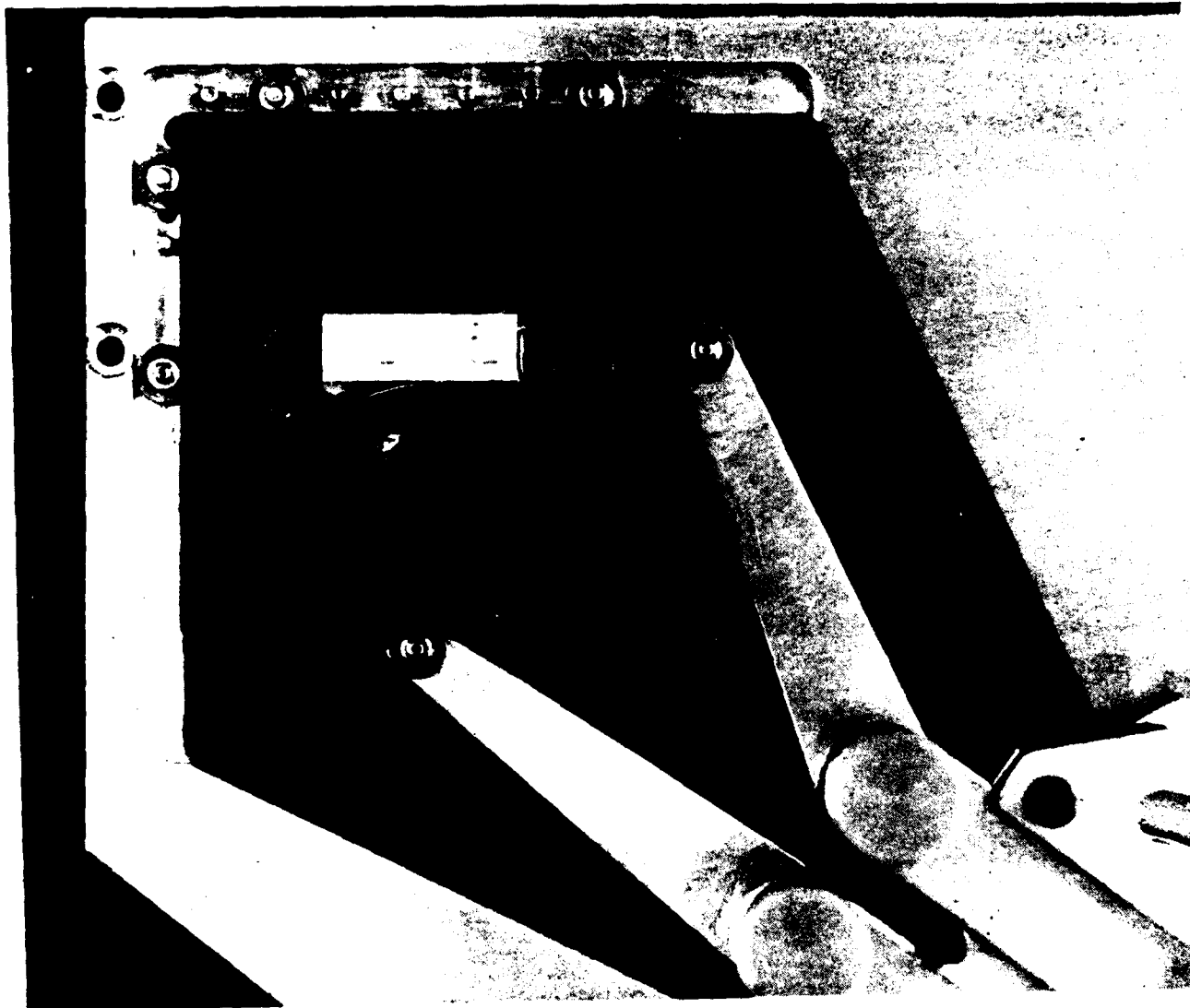
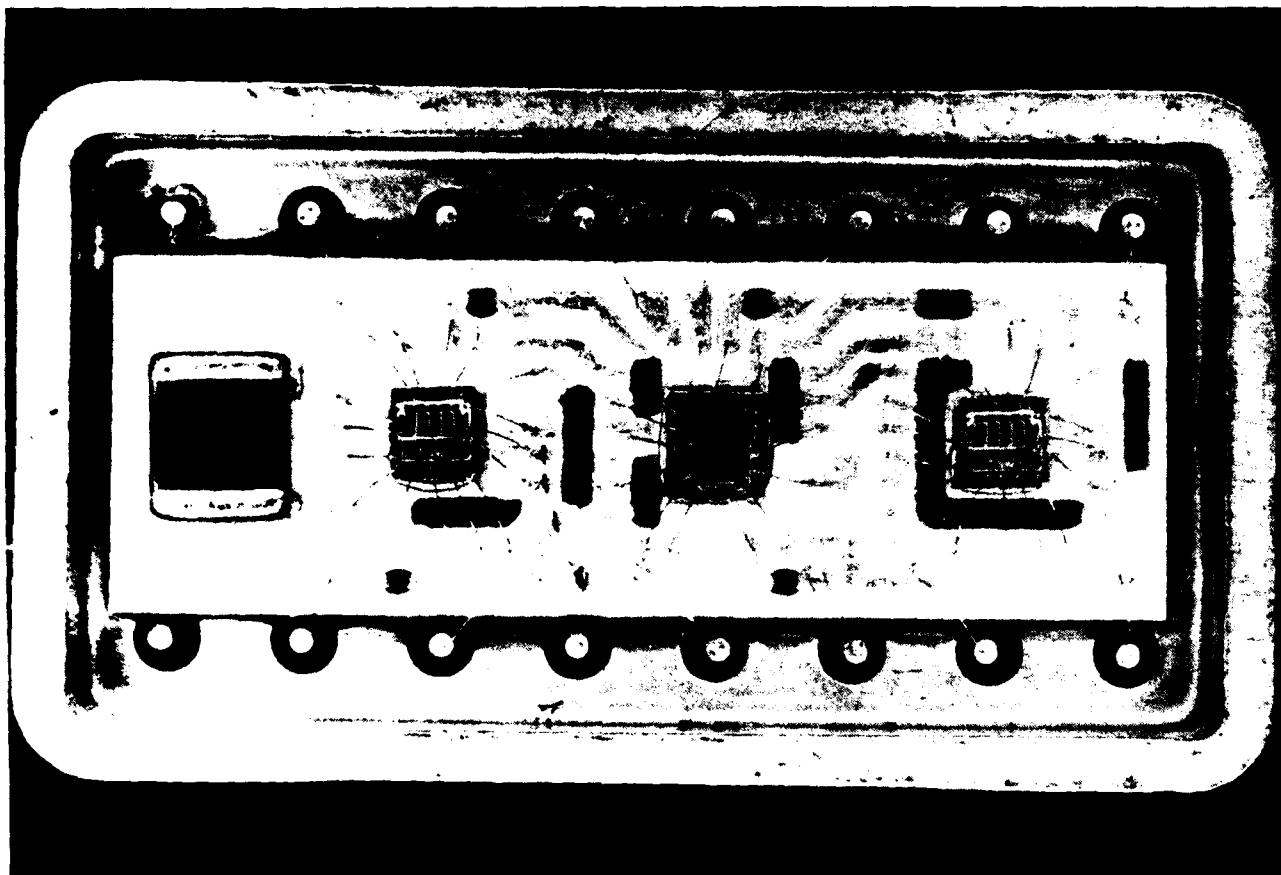


Figure 3-7. Break-up of 2x2 Substrate



*Figure 3-8. Single Substrate in OLB Holder*



*Figure 3-9. Wire Bonded Sync Counter*

## Section 4

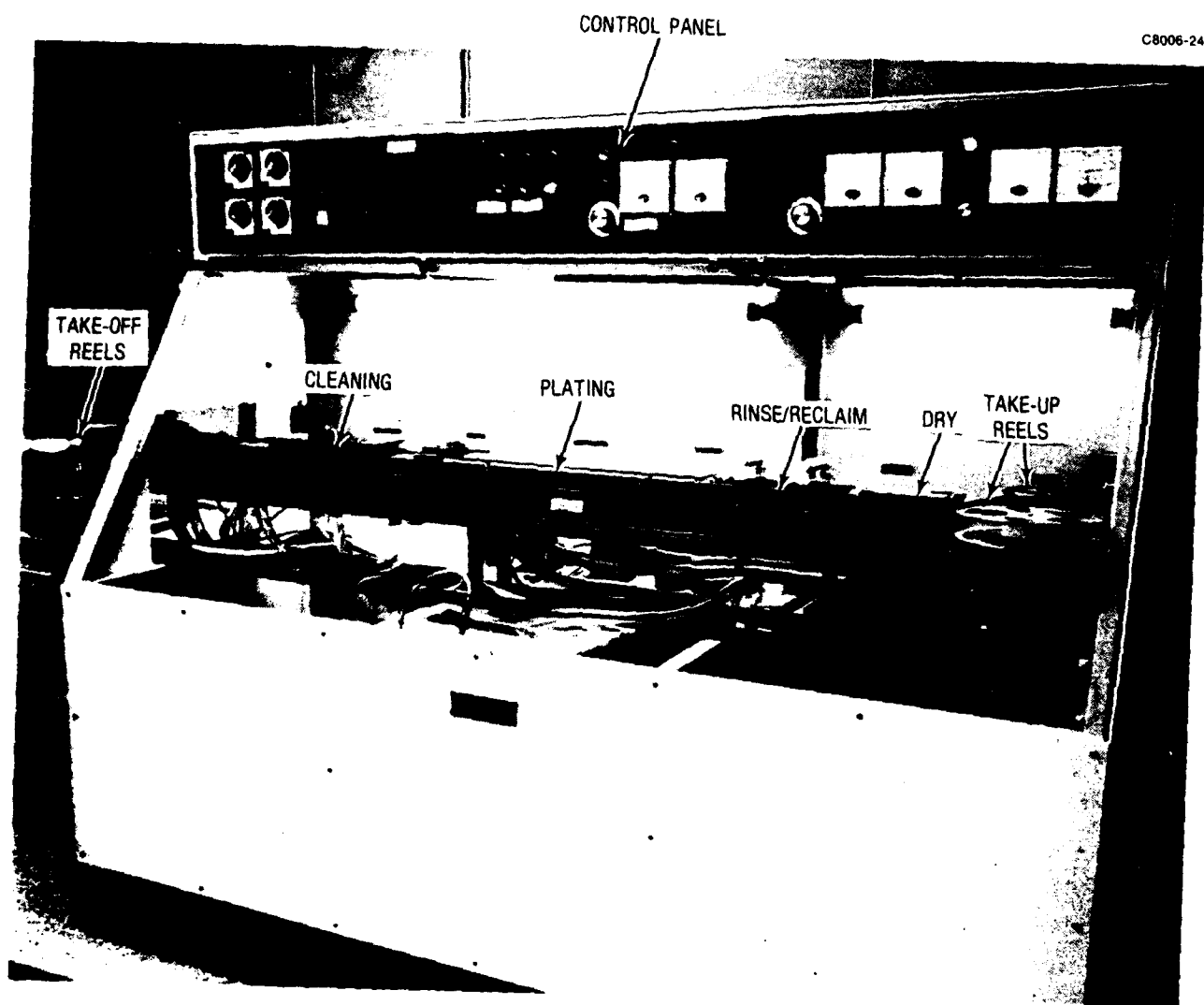
### TAPE MANUFACTURE/PURCHASING

Lead frame tape (Figure 4-1) has been available to AvD from our LISD plant in Phoenix, where automatic equipment exposed and etched the purchased laminate (copper on prepunched polyimide). Approximately 10,000 frames have been produced during the course of this program. Because the LISD facility is set up to produce production quantities, no supply problems have been experienced. All tape used for this program is three-layer, 35mm wide polyimide, laminated to one ounce of electro deposited copper. All tape produced in Phoenix was plated with approximately 100 microinches of gold on the newly designed and installed continuous reel plater in our AvD facility in Clearwater (see Figures 4-2 and 4-3).

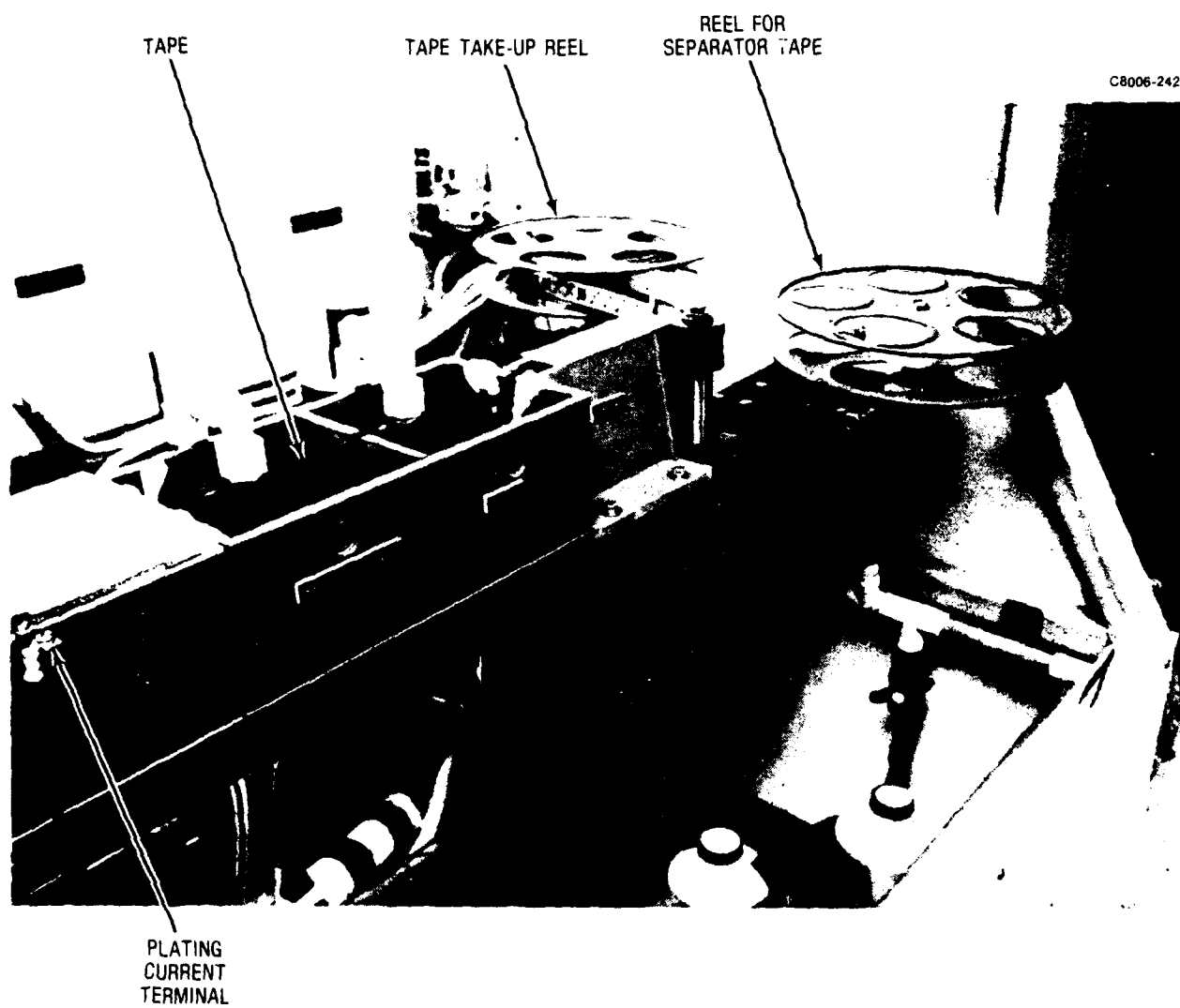




*Figure 4-1. Typical 35mm Lead Frame Tape*



*Figure 4-2. Continuous Tape Plater*



*Figure 4-3. Continuous Tape Plater - Detail*

## Section 5

### WAFERS/CHIPS

Both 54LS161A and 54LS165 chips were purchased from Motorola on the format of 4-inch wafers. Because the processing equipment in Colorado Springs could not handle 4-inch wafers they were cut into quarters prior to processing (see Figure 5-1). Subsequent difficulty in handling this irregular format caused heavy losses at silicon nitride passivation and barrier layer metallization.

Figure 5-2 gives a schematic overview of the processing required and the respective locations of the wafer bumping process.

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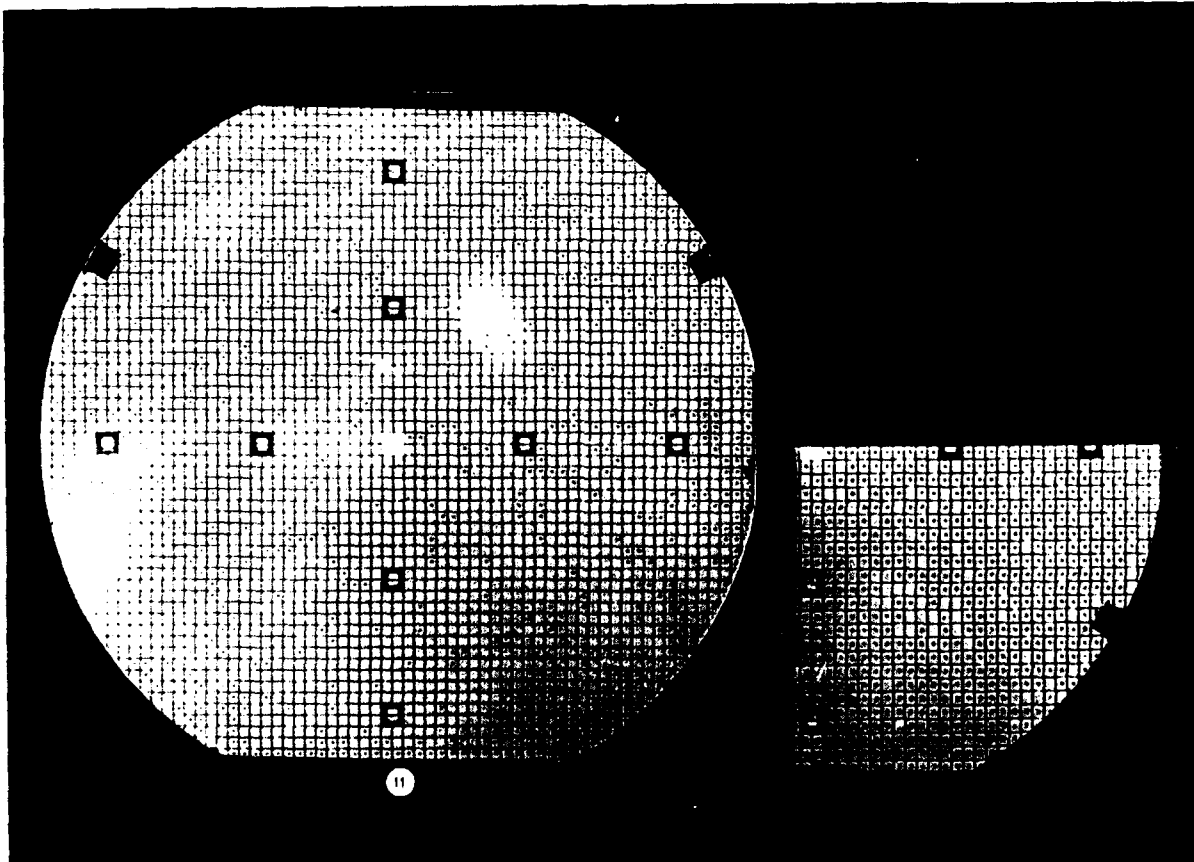


Figure 5-1. 4-inch Wafer/1/4 Wafer

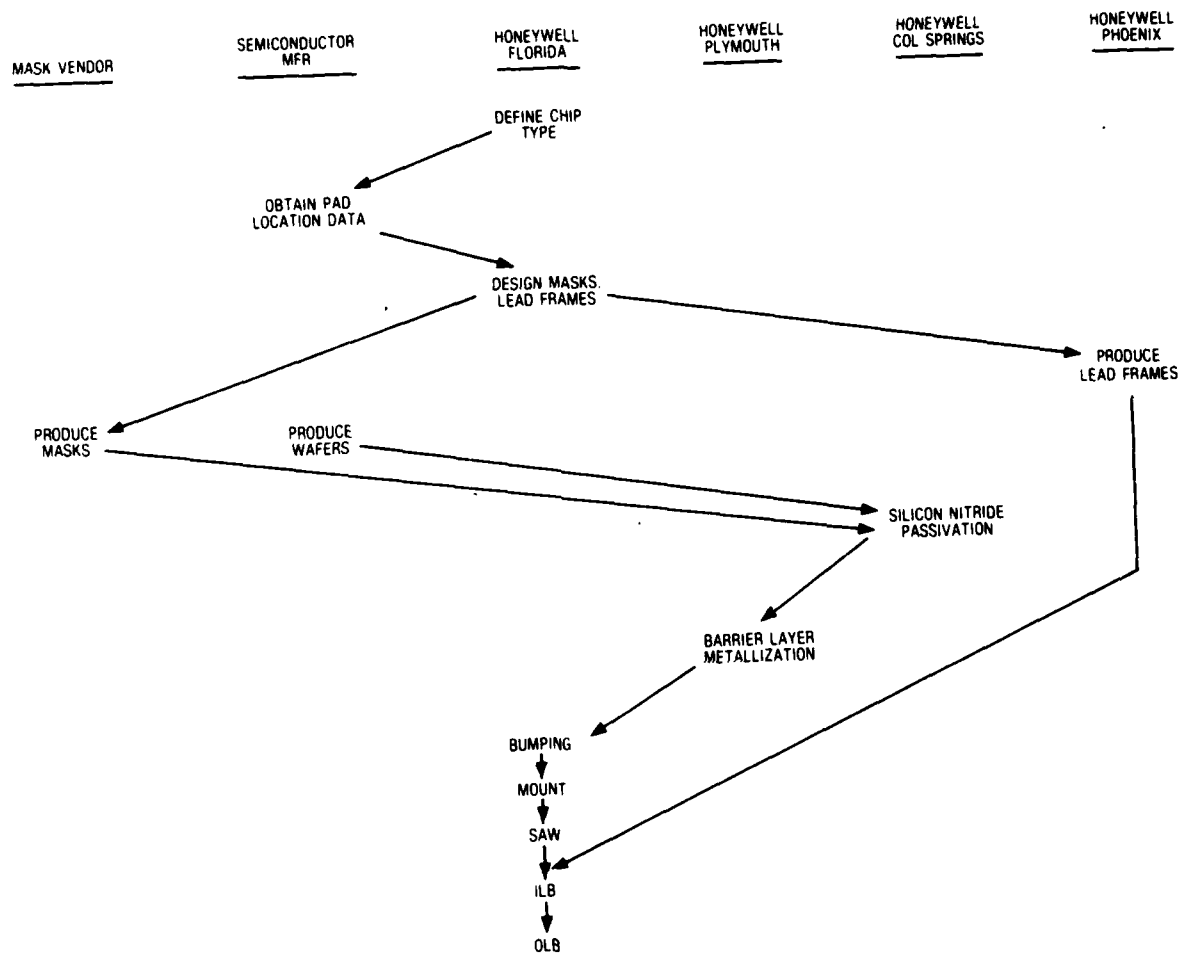


Figure 5-2. TAB Process Location Chart

## Section 6

### DESIGN STANDARDS

The tape was designed per Honeywell Standards (later incorporated into ASTM 7E45 standard for 35mm TAB carrier tape) with 40 leads and 5mm aperture (see Figure 6-1). The OLB pattern was designed per the proposed Honeywell standard (see Figure 6-2). The lead forming profile is shown in Figure 6-3. An enlargement of a 161A chip on tape, prior to OLB, is shown in Figure 6-4, where the exact lead routing is clearly distinguishable.

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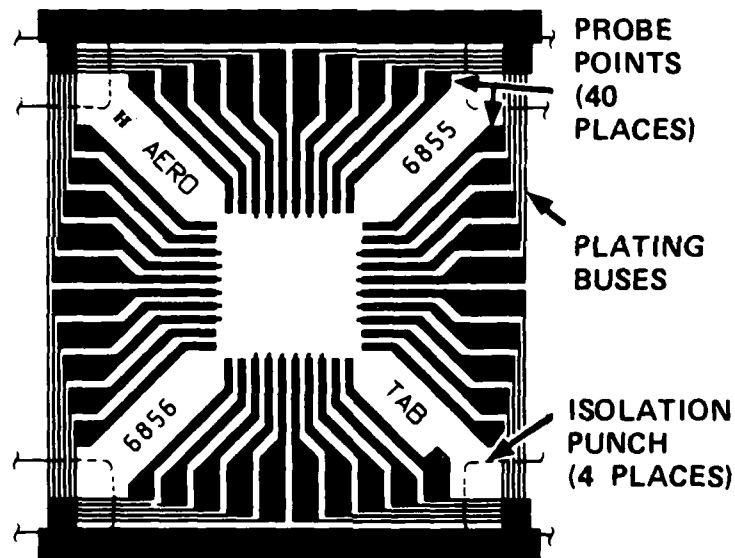
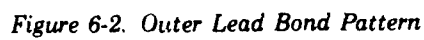
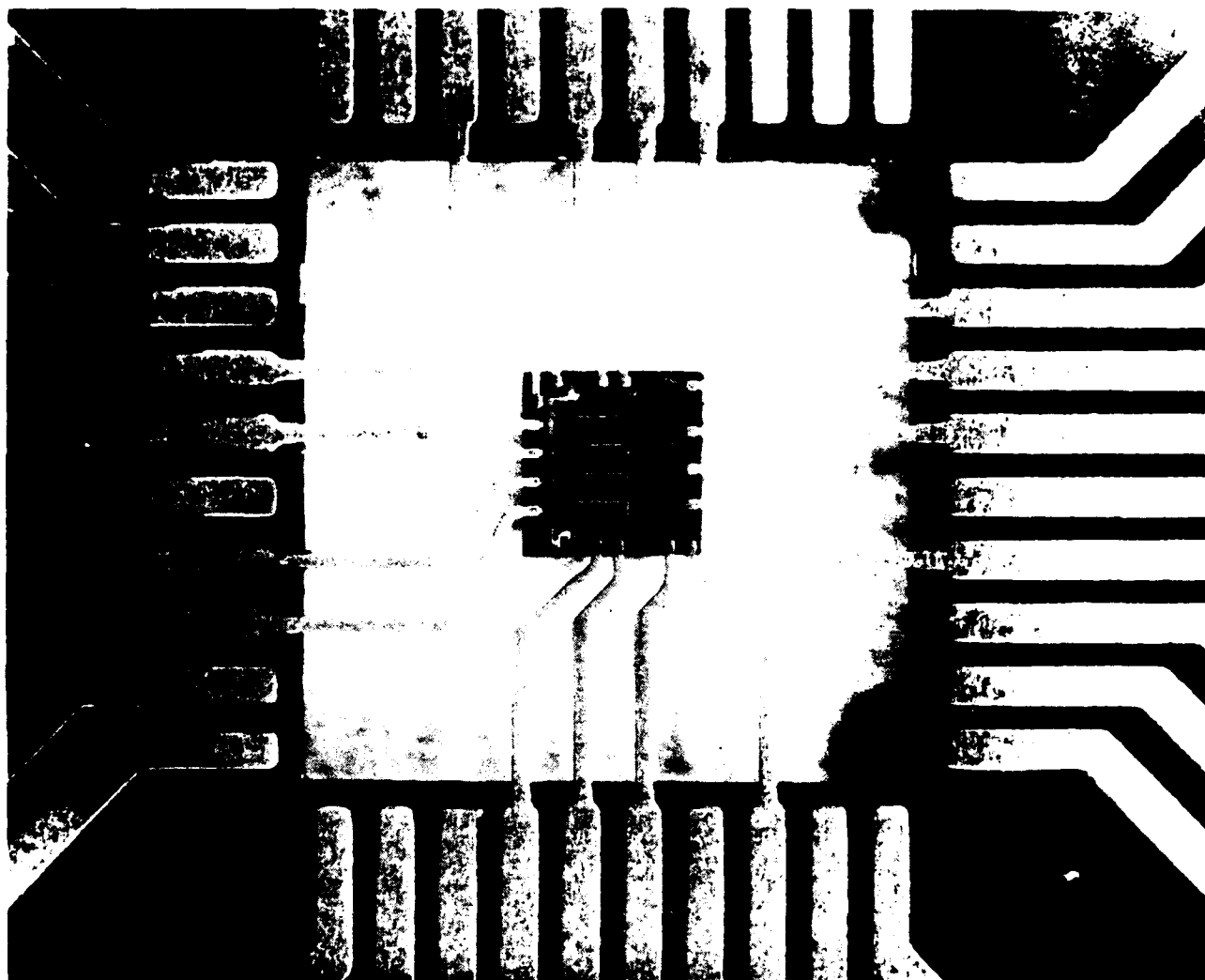


Figure 6-1. Outer Portion of 35mm Tape Frame



**Figure 6-3. Lead Forming Profile**



*Figure 6-4. Close-up of 161A Chip on Tape*



## Section 7

### ELECTRICAL TESTING AND YIELDS

Yield figures are significant indications of the performance of the Sync Counter hybrid as an assembly vehicle to gauge the viability of the TAB-based assembly. Yield figures are derived at four basic operating points in the assembly and test sequence:

1. TAB preparation of wafers/chips and TAB assembly operations
2. Hybrid assembly
3. Visual inspections
4. All electrical tests

An analysis of yields at each of these points has been made and is further discussed in this section.

#### 1. TAB Operations Yields

The TAB operations in this portion of the analysis include barrier layer metallization and bumping, wafer mounting and sawing, Inner Lead Bonding (ILB), electrical test of chips on tape, visual inspection of the chips on individual slide carriers, and finally, Outer Lead Bonding (OLB). Table 7-1 shows these yields for both the 54LS161A and 54LS165 chips.

High losses at wafer barrier layer metallization were caused by the requirement to process quartered 4-inch wafers in equipment set up to automatically handle round 3-inch wafers.

Unusual losses at wafer mounting occurred when the lot of cement turned out to be aged, after a number of quarters were already mounted. These wafers could not be inner lead bonded.

#### 2. Hybrid Assembly Yields

The hybrid assembly yield figure is determined by the ratio of substrates started versus substrates which successfully completed assembly. It therefore includes the OLB bonding operation, except it does not take into account the number of chips, which is shown in the previous section.

Table 7-2 shows the assembly yield on a lot by lot basis. The average assembly yield of all TAB lots was 87.5 percent, the CBI\* lot was 100 percent and the chip and wire lot was 99 percent. The lower TAB assembly yield was caused by the substrate breakage problem, previously described in Section 3.

### 3. Visual Inspections

Visual inspections were carried out at two key points in the assembly sequence. The first, the Pre-Cap Visual inspection took place just prior to seal. The second or Final visual took place just before shipment.

Table 7-3 shows the inspection yields by lot, for each of the two inspection stations. The average yields of the Pre-cap Inspection for the TAB lots was 70.7 percent, for the CBI lot 87 percent and the chip-and-wire lot 86 percent. The relatively low figure for the TAB lots was artificially created by the new and untried TAB accept/reject criteria, which were updated on several occasions. The average yields of the Final Visual Inspection for the TAB lots was 98.9 percent, for the CBI lot 100 percent and for the chip-and-wire lot 94 percent.

### 4. Electrical Test Yields

The most significant information with regard to the success of the TAB approach is obtained through analysis of the electrical test yields. Table 7-4 lists yields per lot for First Electrical test, ATP\*\* at 25°C, -55°C and 100°C as well as total ATP yield for TAB, CBI and chip-and-wire devices. Lot 2 contains data taken both before and after burn-in of the hybrids in order to obtain a yield of the burn-in operation. Analysis of the First Electrical test yield data shown in Table 7-5 clearly shows the significant impact of TAB. The 86 percent yield is obtained because the chips were tested prior to assembly while mounted on tape. The 52 percent yield at the same point, of the conventional chip-and-wire devices, indicates the high losses of the final product mostly due to chips failing to meet operational specification limits. Please note that these chips originated from the same wafer as the TAB chips and were electrically wafer probe tested at the same time. Also significant is the even higher yield of the TAB devices whose chips were not only tested but also burned-in prior to assembly (CBI). This lot has an even higher first test yield of 93 percent due to marginal chips having been stressed and eliminated.

---

\*Chips burned-in prior to assembly.

\*\*Acceptance Test Procedure (Final).

Analysis of the ATP Electrical Tests verify the results with regard to the CBI log. Table 7-6 indicates no significant difference between the TAB and chip-and-wire devices, because the initially unoperative wirebonded chips were culled at the first electrical test. However, the marginally operative devices still escaped and were not eliminated until burn-in, therefore, the CBI lot displays the remarkably high yield of 90 percent at ATP test.

These data demonstrate that test and burn-in of chips on tape is not only feasible, but also highly profitable, and will be further manifested in significant reduction of troubleshooting, repair and retest of assembled devices.

#### 5. Failure Analysis

A failure analysis was performed on a total of six devices. They were various electrical tests done in sequence. With exception of one device all failures were caused by chip processing defects, manifested at first electrical test. The Failure Analysis Report number 66-F covering the analysis in detail is attached as Appendix I to this report.

Table 7-1. Yield History of TAB Operations

<u>Operation</u>		(IC) 161A <u>Qty.</u>	<u>Yield</u> <u>%</u>	(IC) 165 <u>Qty .</u>	<u>Yield</u> <u>%</u>
Metal Bumping	IN:	5,560*		2,421*	
	OUT:	5,280	95 (62.5)*	2,300	95 (58.2)*
Wafer Mount/Saw	IN:	5,280		2,300	
	OUT:	4,600	87.1	2,100	91.3
ILB	IN:	4,600		2,100	
	OUT:	4,270	92.8	2,021	96.2
Elect Test	IN:	4,270		2,021	
	OUT:	3,693	86.5	1,724	85.3
Visual on Carrier	IN:	3,693		1,724	
	OUT:	3,371	91.3	1,596	92.6
OLB	IN:	3,371		1,596	
	OUT:	2,910	86.3	1,355	84.9
Overall Yield*			52.4		56.0

\* Previous experience with metallization and bumping of wafers has shown an approximate 95% yield from those processes. For this reason the quantities of dice shown as the number going "in" are calculated to indicate the number required to provide the number actually yielded coming "out". This was necessary because of the high losses experienced at those two processes due to necessity of manually handling quartered 4 inch wafers on equipment designed to automatically handle 3 inch wafers. The actual yields of 62.5% for 54LS161A chips and 58.2% for 54LS165 chips is substantially typical of the 95% figure which is based on data from processing of about 10,000 chips previously.

The actual number of 54LS161A chips committed to metallization/ bumping in this effort was 8,448 and the number of 54LS165 chips was 3,946.

Table 7-2. Yield History of TAB Operations

<u>Lot No.</u>		<u>Assembly</u>
0001	In	126
	Out	118
	Yield	94%
0002	In	126
	Out	111
	Yield	88%
0003	In	84
	Out	53
	Yield	63%
0004	In	126
	Out	81
	Yield	64%
0005	In	126
	Out	86
	Yield	68%
0006	In	126
	Out	86
	Yield	68%
0007	In	126
	Out	112
	Yield	89%
0008	In	126
	Out	112
	Yield	89%
0009	In	126
	Out	122
	Yield	97%
0010	In	126
	Out	122
	Yield	97%
0011	In	126
	Out	122
	Yield	97%

Table 7-2. Yield History of TAB Operations (Continued)

<u>Lot No.</u>		<u>Assembly</u>
0012	In	73
	Out	73
	Yield	100%
0013	In	126
	Out	122
	Yield	97%
0014	In	31
	Out	31
	Yield	100%
CBI	In	84
	Out	84
	Yield	100%
Chip/Wire		155
		152
		98%

Table 7-3. Yield History of TAB Operations

<u>Lot No.</u>		<u>Visual Inspection</u>	<u>Ext. Visual Final Inspection</u>
0001	In	118	91
	Out	64	91
	Yield	54%	100%
0002	In	111	85
	Out	94	83
	Yield	85%	98%
0003	In	53	39
	Out	38	39
	Yield	72%	100%
0004	In	81	52
	Out	57	51
	Yield	70%	98%
0005	In	86	50
	Out	26	50
	Yield	30%	100%
0006	In	89	66
	Out	69	64
	Yield	77%	97%
0007	In	112	73
	Out	73	73
	Yield	65%	100%
0008	In	126	82
	Out	78	82
	Yield	62%	100%
0009	In	122	98
	Out	90	98
	Yield	74%	100%
0010	In	122	77
	Out	57	77
	Yield	47%	100%
0011	In	122	73
	Out	85	73
	Yield	70%	100%

Table 7-3. Yield History of TAB Operations (Continued)

<u>Lot No.</u>		<u>Visual Inspection</u>	<u>Ext. Visual Final Inspection</u>
0012	In	73	56
	Out	73	54
	Yield	100%	96%
0013	In	122	81
	Out	106	81
	Yield	87%	100%
0014	In	31	23
	Out	31	22
	Yield	100%	96%
CBI	In	84	69
	Out	73	69
	Yield	87%	100%
Chip/Wire		153	66
		132	62
		86%	94%



Table 7-4. Yield History of TAB Operations

Lot No.		1st Electrical Test	Final Electrical Test Yields			Total Yield	Shipped
			ATP** @25°C	ATP @-55°C	ATP @100°C		
0001	In	118	96	92	91		37
	Out	99	92	91	91		
	Yield	84%	96%	99%	100%	95%	
0002	In	111	89	86	86		35
	Out	94	86	86	85		
	Yield	85%	97%	100%	99%	96%	
0003	In	53	47	45	44		39
	Out	47	45	44	39		
	Yield	89%	96%	98%	89%	83%	
0004	In	81	61	57	56		37
	Out	62	57	56	52		
	Yield	76%	93%	98%	93%	85%	
0005	In	86	76	66	65		50
	Out	77	66	65	50		
	Yield	89%	87%	99%	77%	66%	
0006	In	89	72	71	69		65
	Out	72	71	69	66		
	Yield	81%	99%	97%	96%	92%	
0007	In	112	89	89	81		73
	Out	90	89	81	73		
	Yield	80%	100%	91%	90%	80%	
0008	In	125	114	112	106		82
	Out	116	112	106	82		
	Yield	93%	98%	95%	77%	72%	
	In		94	90	90		
	Out		90	90	89		
	Yield		96%	100%	99%	95%	

\*Pre burn-in results Lot 0002

\*\*Acceptance Test Procedure

Table 7-4. Yield History of TAB Operations

Lot No.		1st Electrical Test	Final Electrical Test Yields			Total Yield	Shipped
			ATP @25°C	ATP @-55°C	ATP @100°C		
0009	In	122	109	109	105		98
	Out	110	109	105	98		
	Yield	90%	100%	96%	93%	90%	
0010	In	122	104	104	103		77
	Out	106	104	103	77		
	Yield	87%	100%	99%	75%	74%	
0011	In	122	107	104	100		73
	Out	107	104	100	73		
	Yield	88%	97%	96%	73%	68%	
0012	In	73	67	65	63		56
	Out	67	65	63	56		
	Yield	92%	97%	97%	89%	84%	
0013	In	122	95	93	84		81
	Out	101	93	84	81		
	Yield	83%	98%	90%	96%	85%	
0014	In	31	27	26	26		23
	Out	27	26	26	23		
	Yield	87%	96%	100%	88%	85%	
CBI	In	84	77	73	72		69
	Out	78	73	72	69		
	Yield	93%	95%	99%	96%	90%	
Chip/ Wire*	In	153	73	73	71		64
	Out	80	73	71	66		
	Yield	52%	100%	97%	93%	90%	
	In		80	75	74		
	Out		75	74	73		
	Yield		94%	99%	99%	91%	

\*Pre burn-in results chip/wire.

Table 7-5. First Electrical Test Yields

	<u>Qty In</u>	<u>Rej</u>	<u>Acc</u>	<u>Yield (%)</u>
TAB	1367	192	1175	86
C/W	153	73	80	52
C.B.I.	84	6	78	93

Table 7-6. ATP Test Yields

	<u>Qty In</u>	<u>Rej</u>	<u>Acc</u>	<u>Yield (%)</u>
TAB	1158	212	946	82
C/W	80	14	66	83
C.B.I.	77	8	69	90

## Section 8

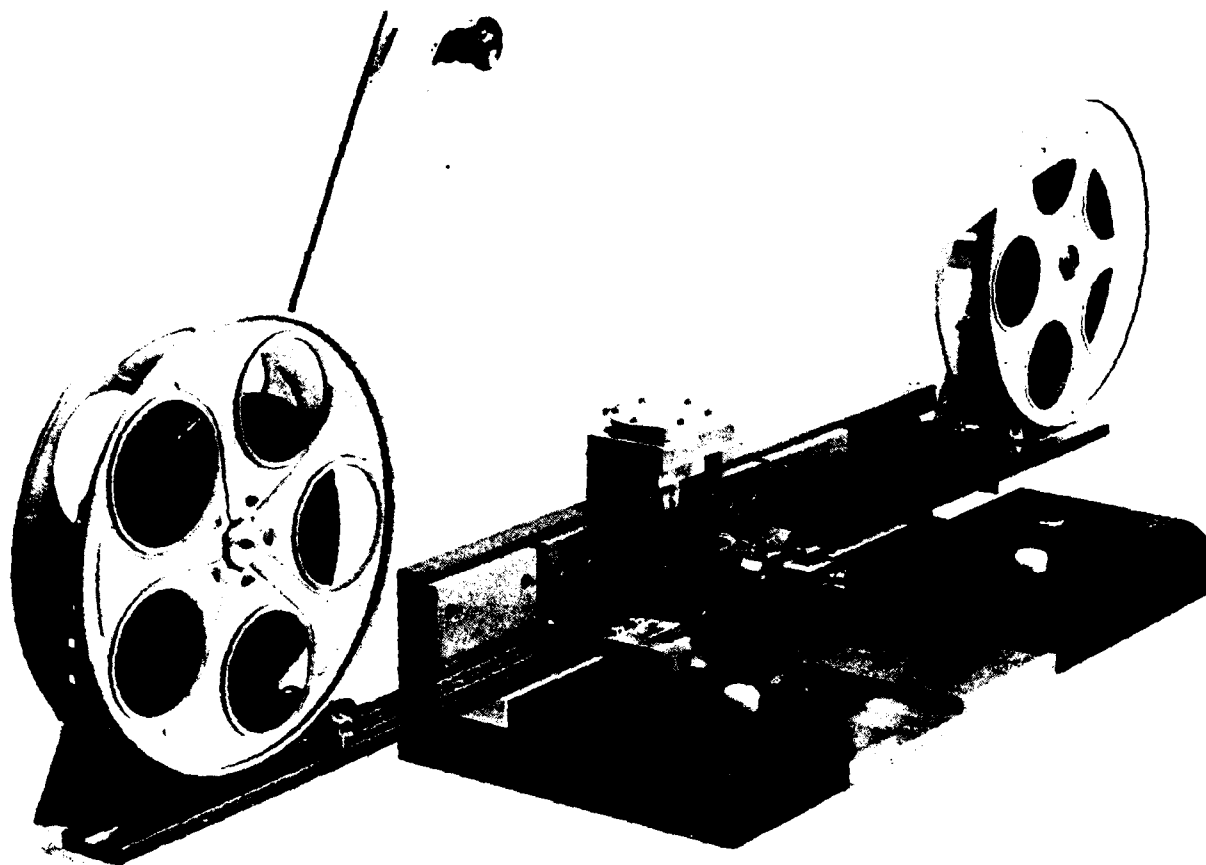
### EQUIPMENT

The following TAB equipment and fixtures were used in the manufacturer of the Sync Counter hybrid microcircuit.

- Continuous Tape Plater - Model No. STP, Microplate Inc. Used for reel-to-reel gold plating of copper lead frame material (see Figures 4-2 and 4-3).
- Inner Lead Bonder - Model I-1000, The Jade Corp. Used to bond all chips to the lead frame tape (see Figure 8-1).
- Manual Tape Test Handler - Model 001, The Jade Corp. Used to contact the chips on lead frame tape while electrically testing chips on the Fairchild 5000 (see Figure 8-2).
- Lead Frame Cutting Machine - Model IIB, Seary Mfg Corp. Used to cut the lead frame tape into individual frames in preparation for slide carrier mounting (see Figure 8-3).
- Framing Fixture - Model ME80C475, Honeywell Inc. Used to mount individual lead frames in standard slide carrier (see Figure 8-4).
- Burn-In Tank - Model PSK 2922, Honeywell Inc. Used to burn-in chips on tape after ILB but prior to OLB (see Figure 8-5).
- Automatic Test Handler for Slide mounted tape frames (in Manual Mode) - Model 5311, The Jade Corp. Used to test chips on tape after burn-in (see Figure 8-6).
- Outer Lead Bonder - Model 4810, The Jade Corp. Used to excise, form, place and bond chip leads on the hybrid substrate (see Figure 8-7).
- Automatic Test Handler for Slide Mounted frames, Model 5311/S/N 1, the Jade Corp. (see Figure 8-8).



*Figure 8-1. Inner Lead Bonder (ILB) Jade I-1000*

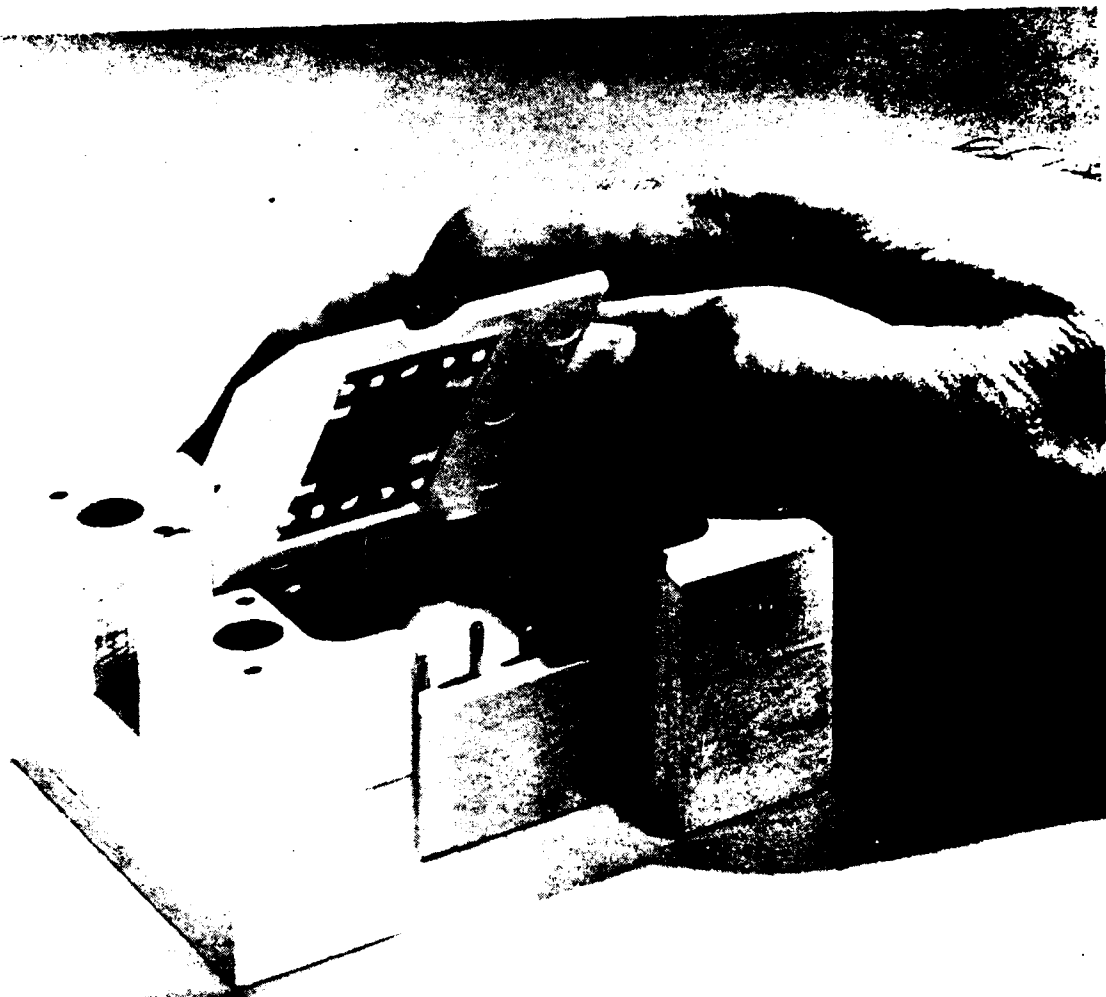


*Figure 8-2. Manual Reel-to-Reel Tester Jade Model-001*

A8010-063

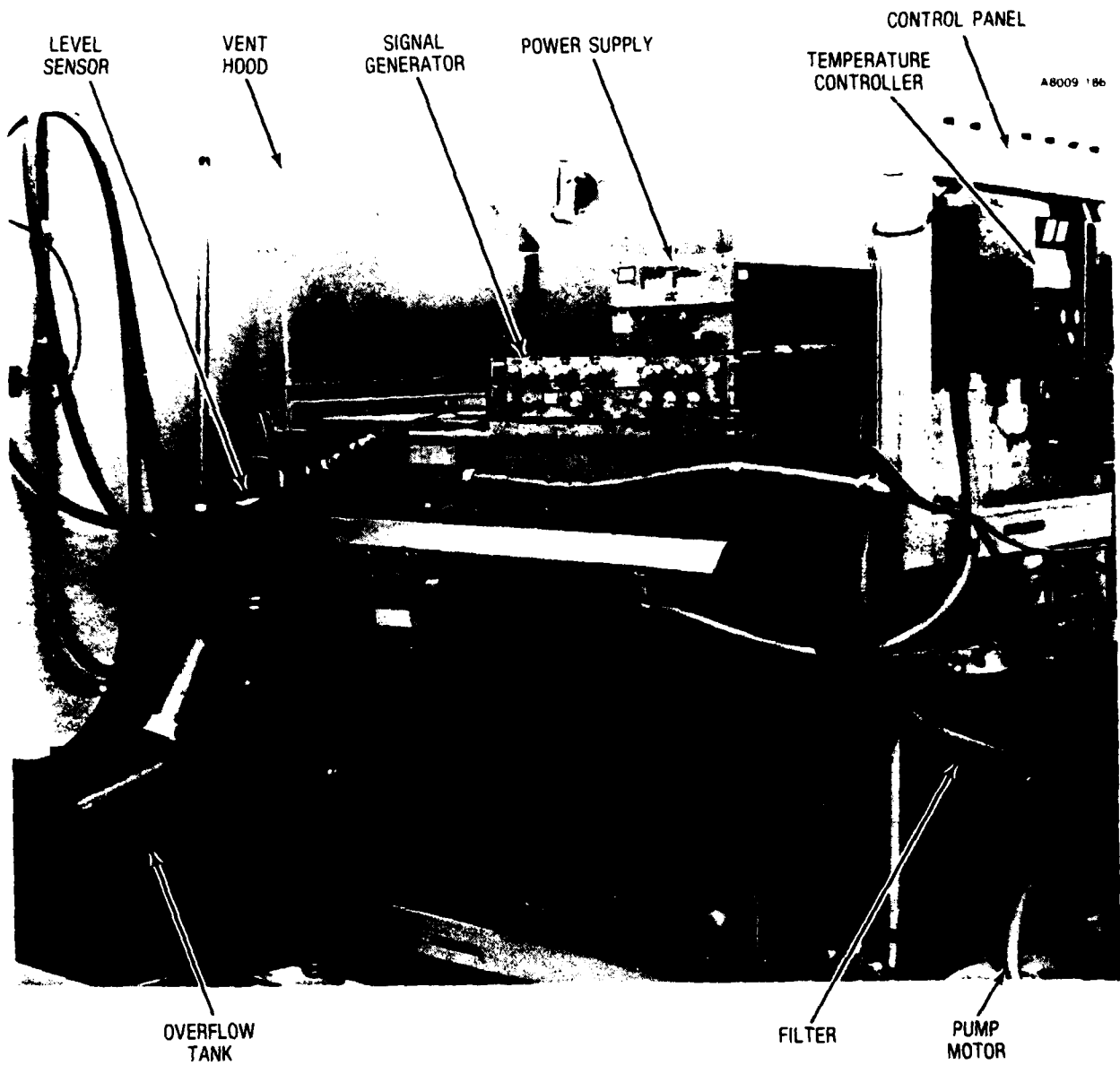


Figure 8-3. Lead Frame Cutter

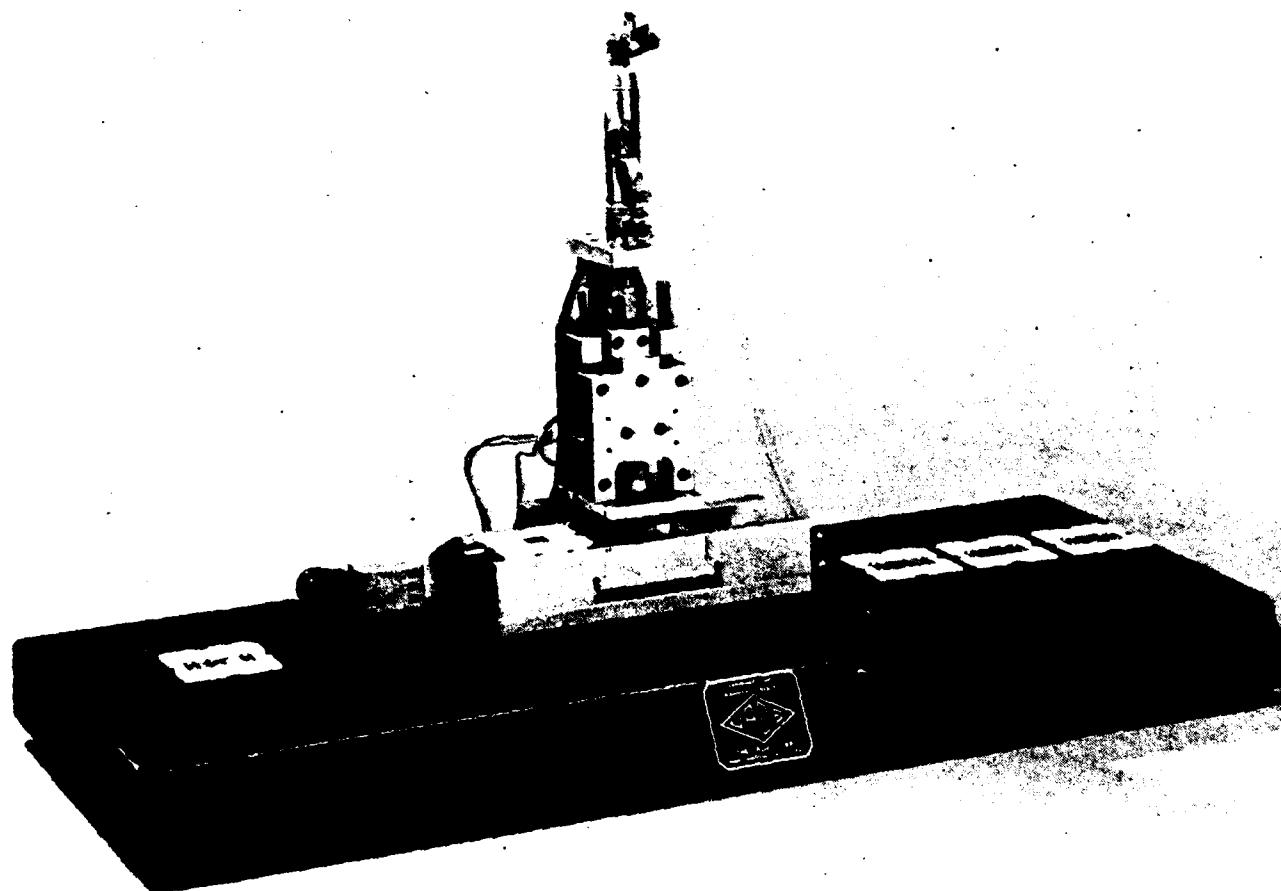


*Figure 8-4. Framing Fixture*

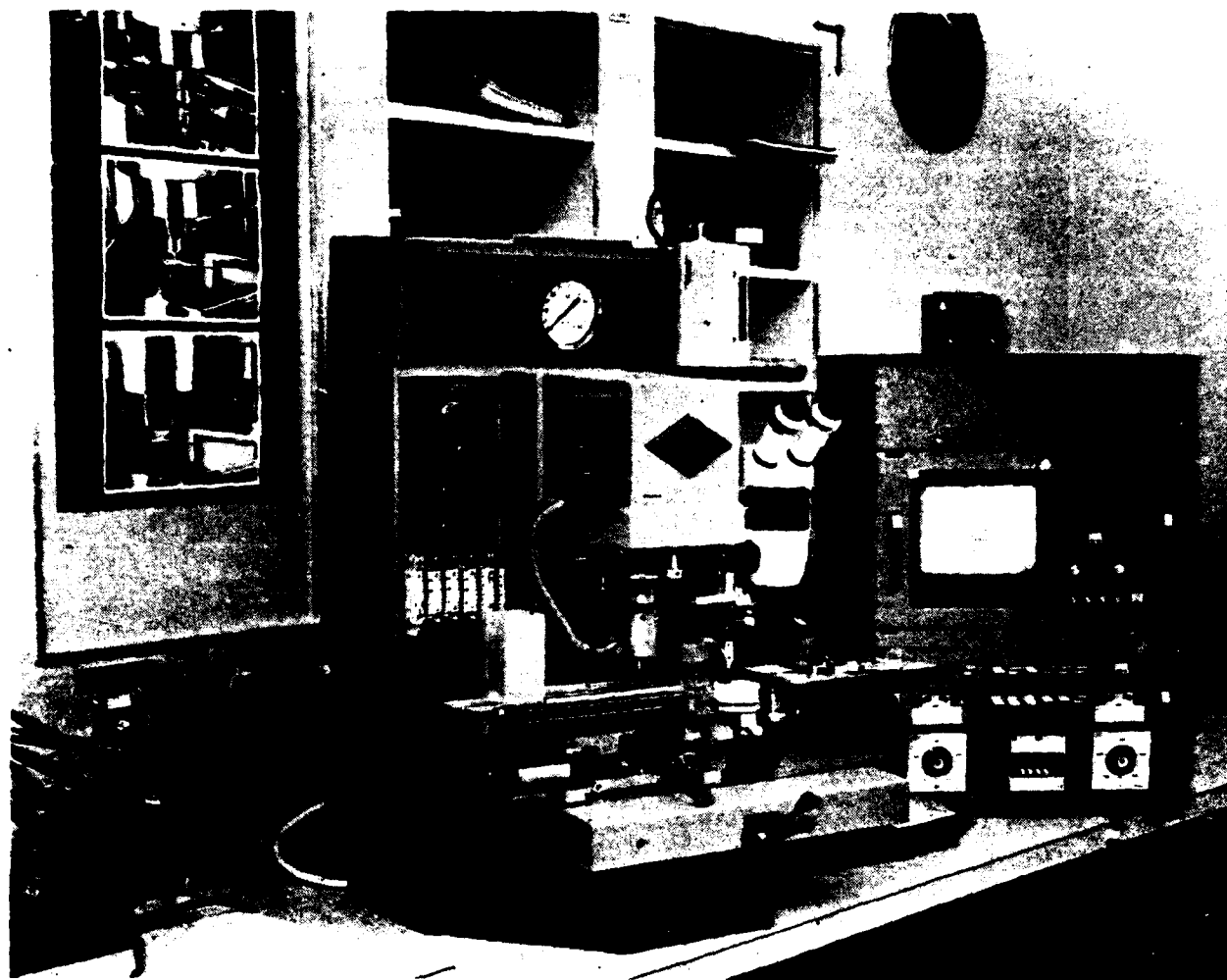




*Figure 8-5. Burn-in Tank*



*Figure 8-6. New Slide Tester on Temporary Base*



*Figure 8-7. Jade 4810 Outer Lead Bonder*



*Figure 8-8. Automatic Test Handler for Slide  
Mounted Tape Frames Jade 5311*

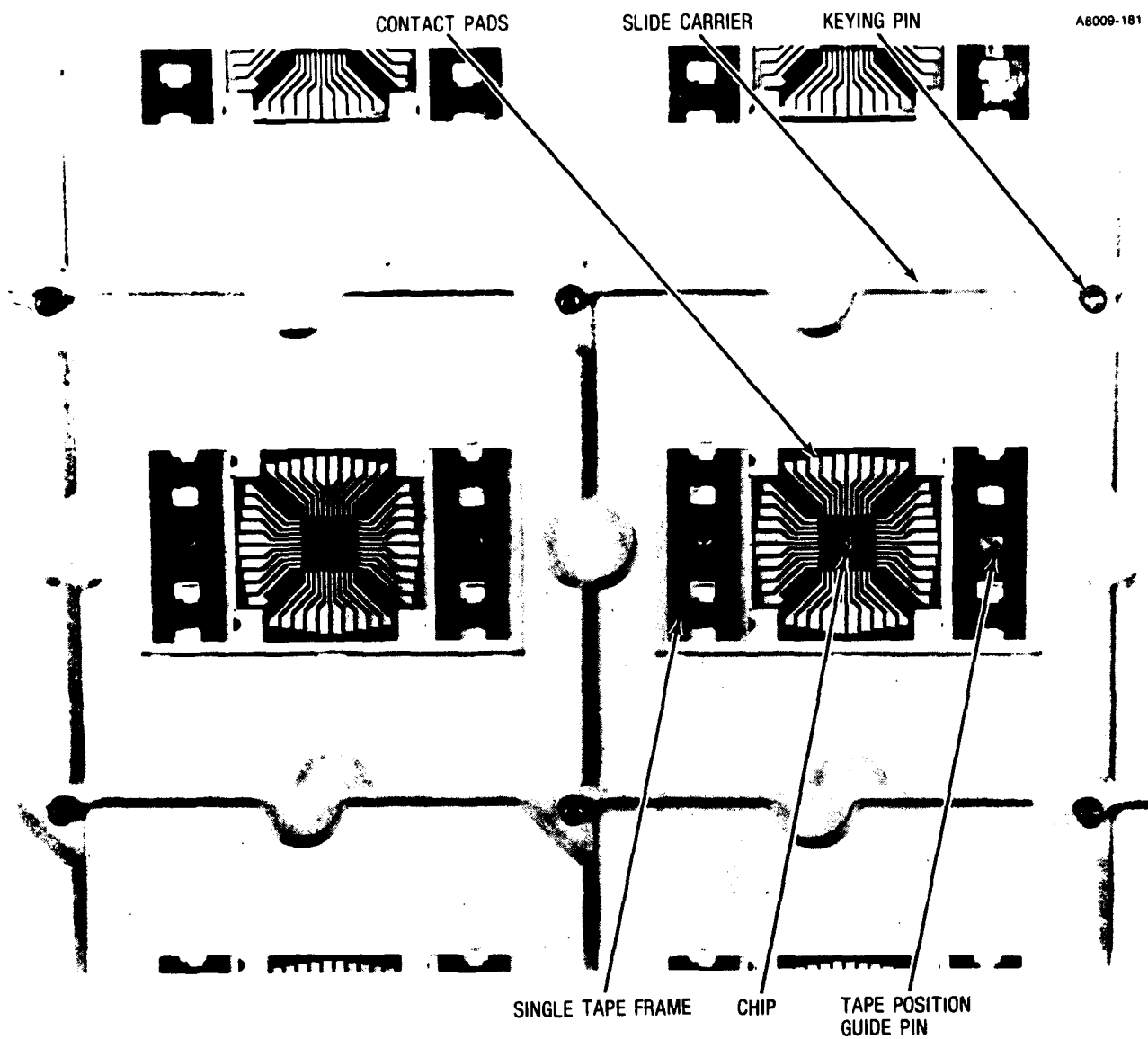
## Section 9

### BURN-IN

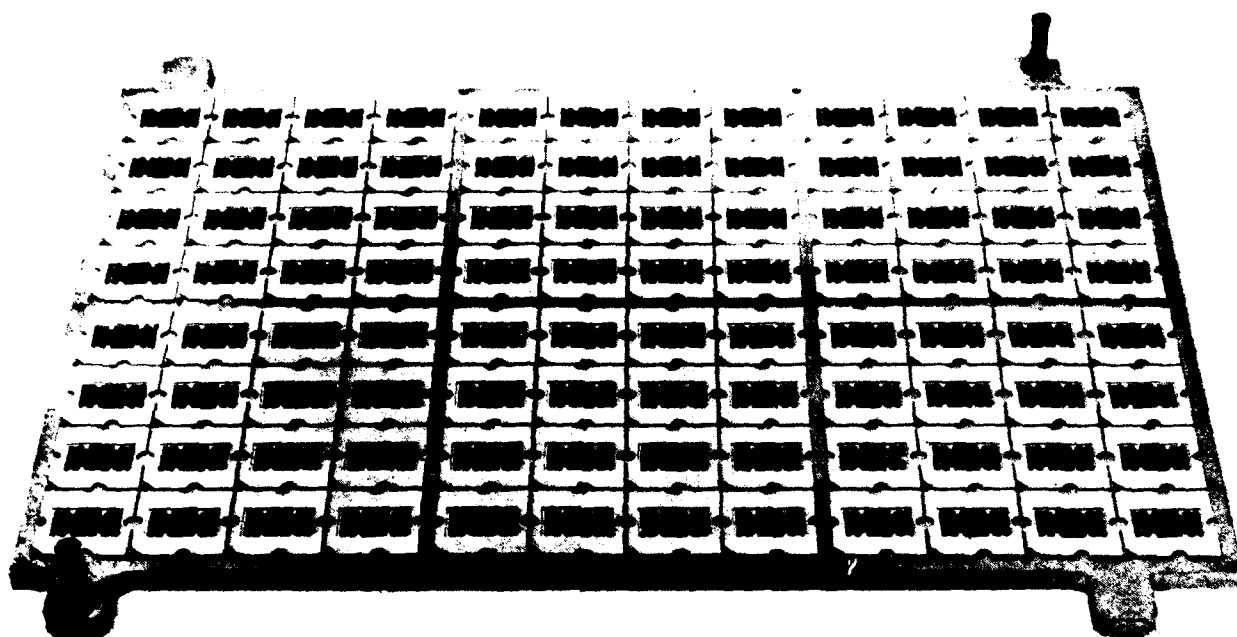
When burn-in is required for hybrid devices, they are normally subjected to this screen after completion of the entire assembly process. Burn-in of individual semiconductor chips and other components prior to assembly has not been practical. TAB technology made it possible to burn-in semiconductor chips prior to assembly, as they are electrically accessible on the tape. Because the burn-in screen is most effective for semiconductor parts, applying this screen to the chips prior to assembly may, in many cases, alleviate the need for burning in the complete hybrid after assembly. Most importantly, however, it will reduce the amount of rework required after first electrical test.

The burn-in tank consists basically of an insulated reservoir filled with FC-43 which is heated, filtered and slowly circulated (see Figure 8-5). The slide carriers containing single tape frames with one chip each (Figure 9-1) are positioned on a tray having 96 positions (see Figure 9-2). The tray is married to an interconnect/contact board containing POGO pins to contact the lead frame pads (see Figure 9-3). Figure 9-4 shows a close-up of the interconnect board with the spring loaded POGO pins and the aperture allowing free flow of fluorocarbon over the chip. The completed tray assembly (Figure 9-5) is then lowered into the tank and remains there for the required period (usually 168 hours), while the fluorocarbon is heated to the desired temperature, usually 125°C. Electrical signals to operate each device are fed into the tray through a connector assembly. Upon completion of the required burn-in time, the tray is removed and disassembled. The individual chips-on-tape then undergo electrical testing. The system can be adapted to burn-in any chip type by changing the 24 plug-in interconnect boards (Figure 9-6) each of which is designed to power a specific chip type.

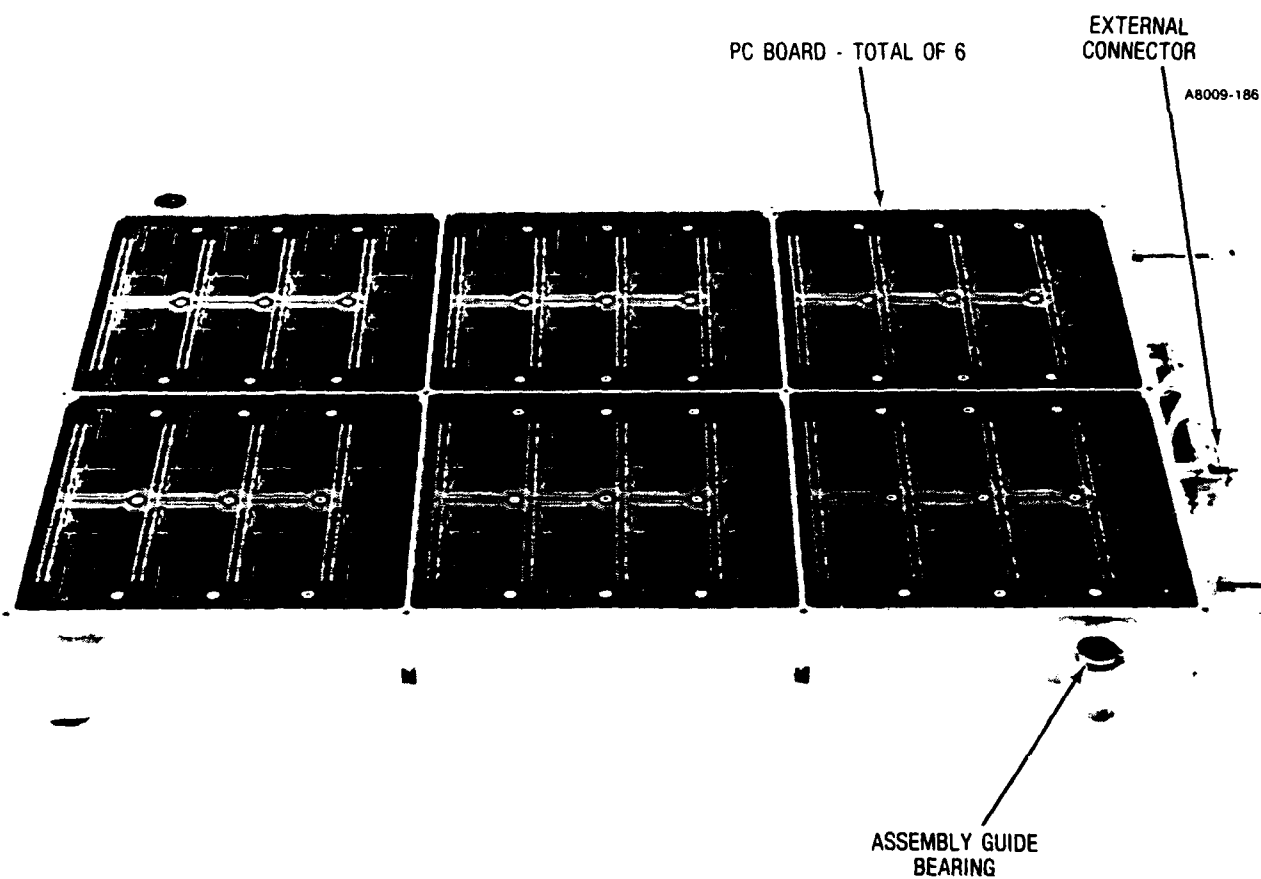
Eighty-four circuits were fabricated from chips which had been burned in for 168 hours at 125°C. Because of a malfunction in the Test Handler, the chips could not be electrically tested following burn-in but all available burned-in chips on tape were committed to circuits. Yields from this lot are shown in Table 7-4 as lot number "CBI". As can be seen, the Total Yield of 90% was comparable to yields from other lots and would probably have been significantly higher had testing of chips on tape following burn-in been possible.



*Figure 9-1. Chip on Single Frame Mounted in Slide Carrier*



*Figure 9-2. Burn-in Tray Populated with 96 Slide Carriers Prior to Assembly*



*Figure 9-3. Interconnect Board Assembly*



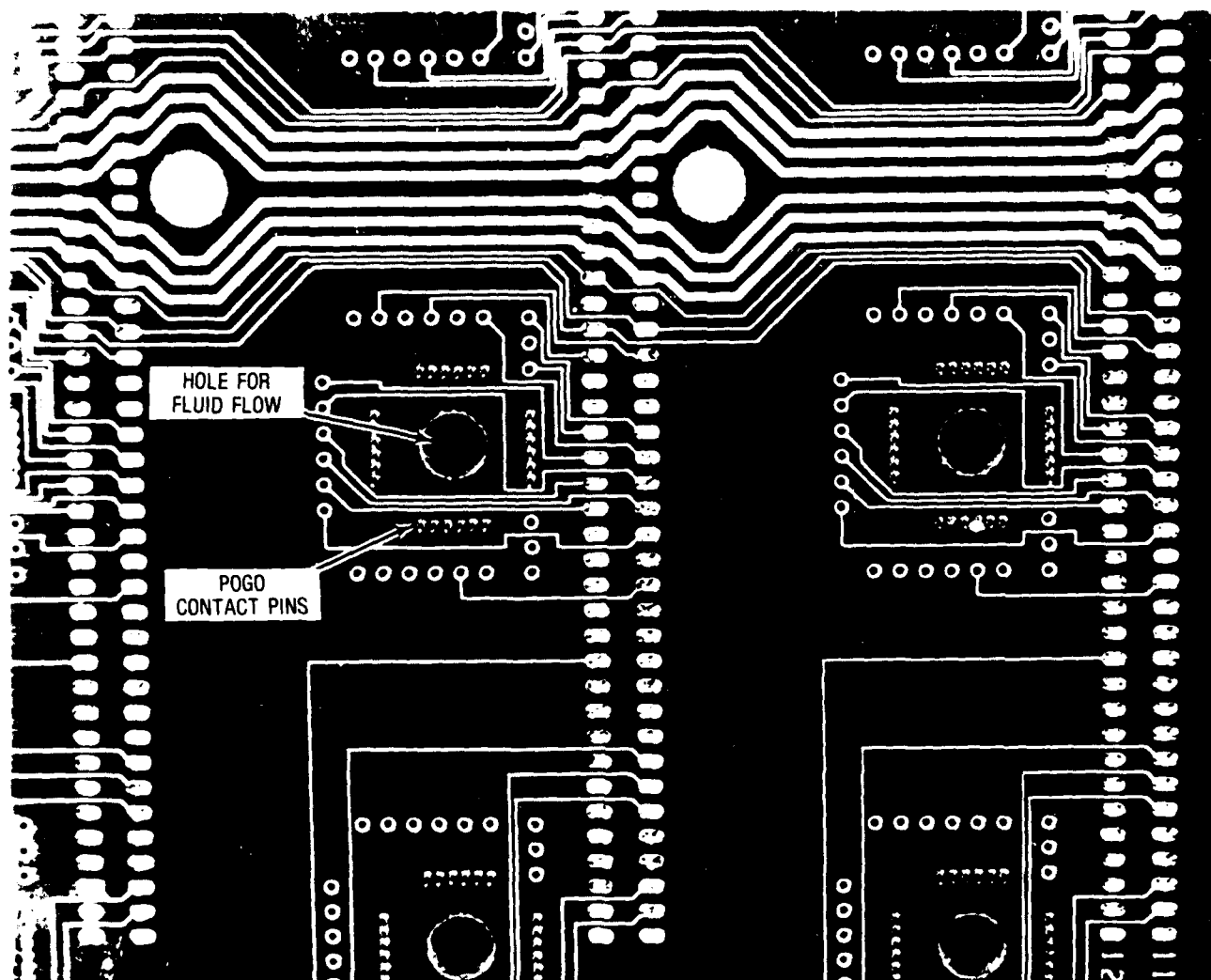
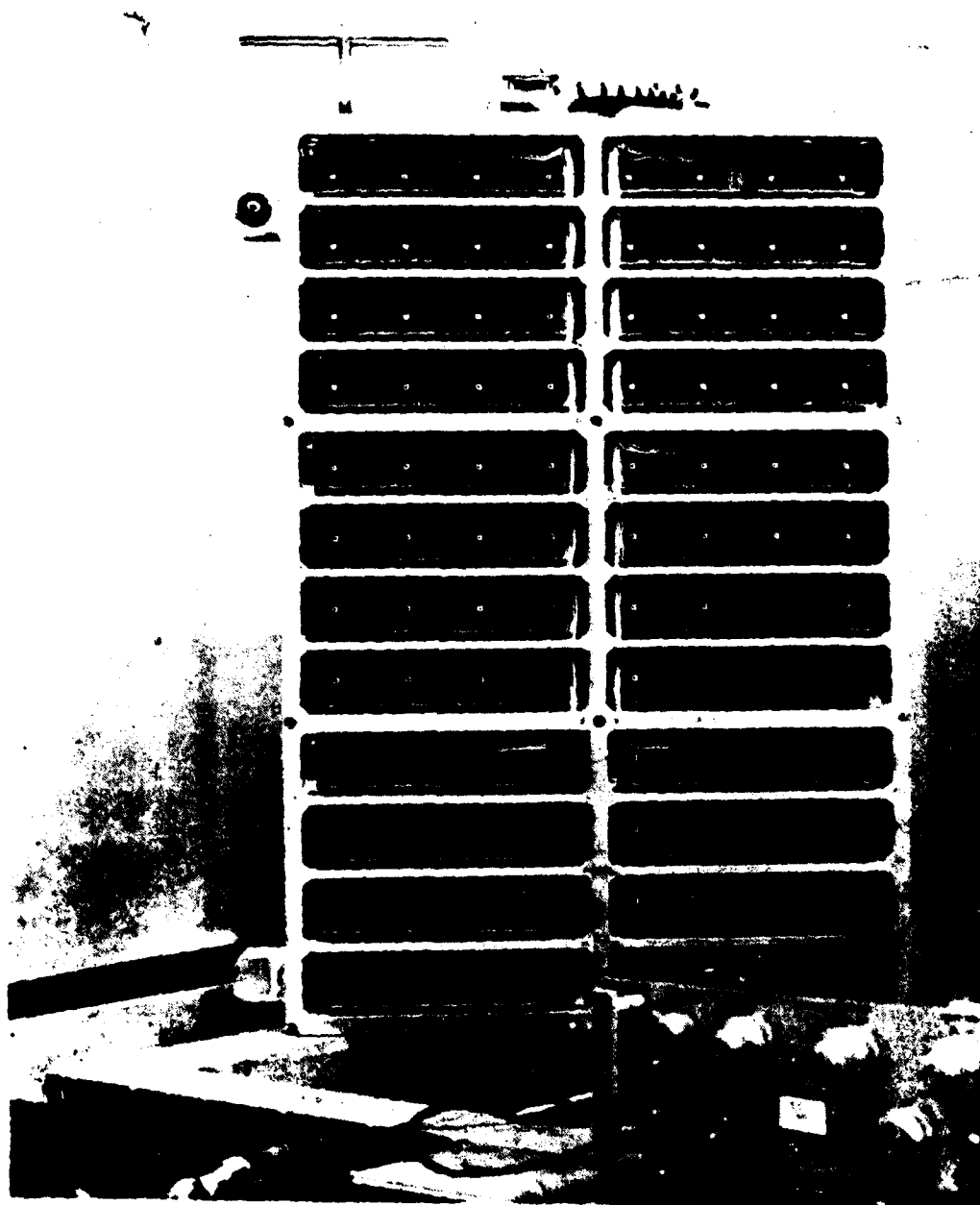
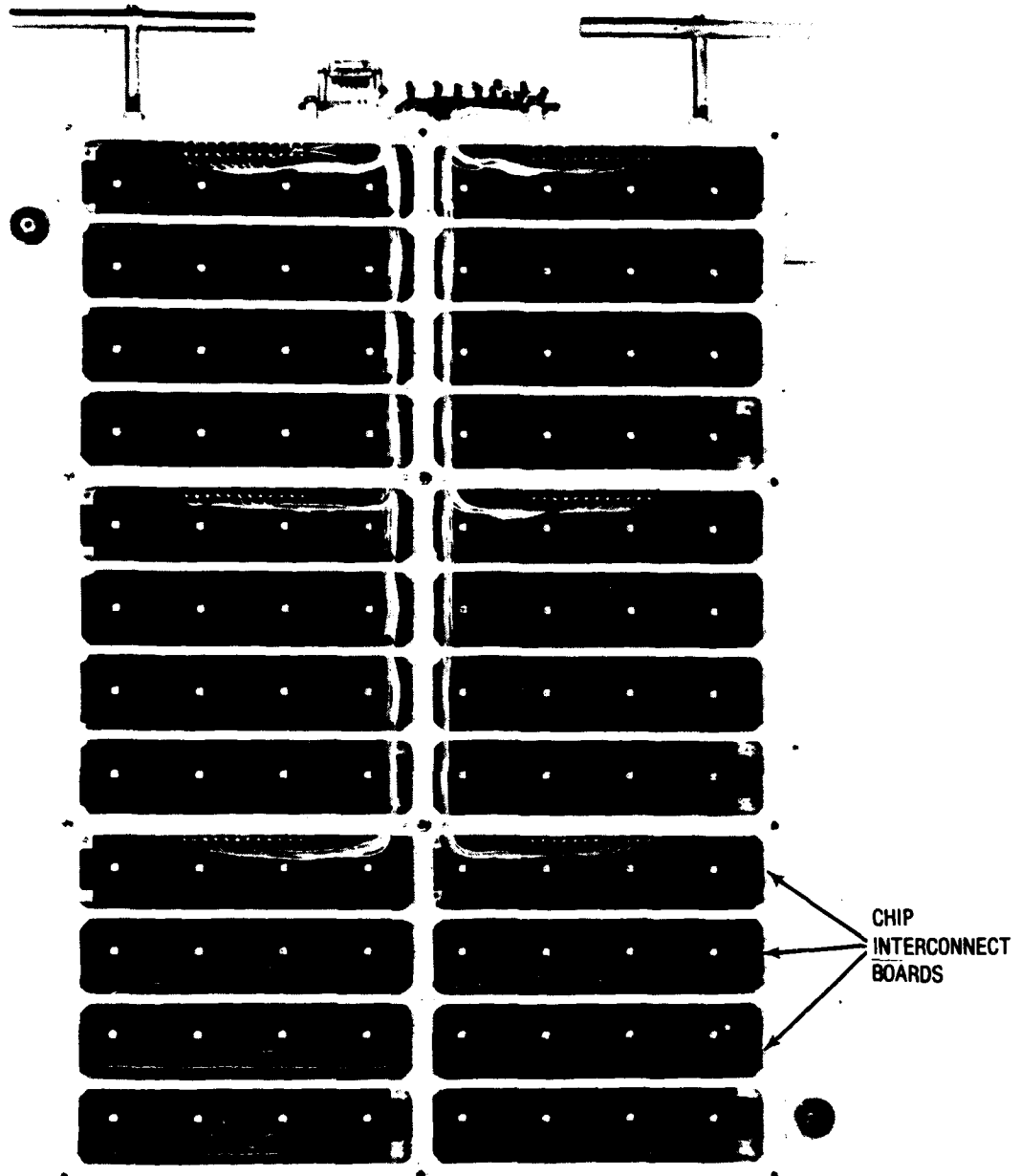


Figure 9-4. Interconnect PC Board Detail



*Figure 9-5. Loaded and Assembled Tray Ready For  
Insertion in Fluid*



*Figure 9-6. Burn-in Tray With Vertical Chip  
Interconnect Board*

## Section 10

### QUALIFICATION

The TAB E/M Sync Counter hybrid has been subjected to a military-type qualification program, which has tested every aspect of the performance capability of the device. With relatively minor exceptions the TAB hybrid has passed these qualification tests in a truly remarkable way.

The qualification program, including prior environmental screening steps is shown in detail on Figure 10-1. The qualification program consisted of five basic elements as follows: (Figure 10-2)

1. A qualification test program based on the Patriot Fuze Program requirements and imposed by U.S. Army ERADCOM for the completed hybrid devices.
2. A stringent qualification program as required by the USAF B-52 retrofit program and imposed on Honeywell Hybrid devices.
4. Qualification of materials prior to assembly.
5. Qualification of TAB equipment on a daily basis during assembly.

Items 1 and 2 are based on MIL-STD-883, Method 5008 Group B, C and D testing and are highlighted in Figures 10-1 and 10-3 as ERADCOM/Honeywell tests. The qualification requirements (quantity of devices and limits) are combined into one set of tests. A total of 81 devices were subjected to the different portions of the qualification program. Table 10-1 lists the device serial numbers and their respective lots for each of the Group B, C and D tests.

#### Device Qualification Results

The TAB hybrids have passed all but two of the above listed qualification tests without a single failure.

The first of the two tests failed was the Group B Die Shear Test, in which 2 out of 3 chips in every one of the five packages failed to meet the strength limit. An analysis of the failed epoxy joint indicated a high porosity level in the epoxy, plus the absence of any evidence of contamination (see Analysis Report #V02907, Appendix II). An investigation into the assembly traveller and sequence revealed that the epoxy of several lots had been thinned in unauthorized fashion, and also that several lots of screen printed epoxy had been stored over the week-end prior to die attach (OLB). This could have caused partial curing of the epoxy and resulting low bond strength. It is interesting to note that even with the low strength die bonds, the devices still met all environmental qualification tests, including mechanical, vibration and constant acceleration. This confirms the earlier theoretical analysis (Report #DELET-TR-77-2708-F, September 1979) which indicated that die attach is not required for mechanical integrity in TAB devices.

The above discussed qualification results are considered extremely positive. It appears that the TAB devices are almost indestructible under a variety of environments and stresses.

The qualification test travelers and QIIs (Quality Inspection Instructions) as well as the printed out electrical test results are included in a report titled "Qualification Test Data" and is available at ERADCOM.

#### Material Qualifications

In addition to device (hybrid) qualification tests after assembly and test, qualification on parts and materials was performed prior to use in assembly. These included the following:

1. Substrate qualifications, consisting of thickness profiles, TAB bond tests on the thick film gold, and gold wire bond pull strength tests.
2. Gold Paste Qualification Tests, consisting of adhesion tests and wire bond pull tests to check bondability of the gold.
3. Qualification of epoxies used to bond the chips and capacitor to the substrate.

#### TAB Bond/Equipment Qualification

Prior to and during each day's assembly the TAB bonding equipment was qualified by bonding all leads of one chip followed by pull strength testing. Mean ( $\bar{X}$ ) and standard deviation ( $\sigma$ ) were then calculated. If these values were such that  $\bar{X}-3\sigma$  was equal to or greater than 10 grams the ILB or OLB was qualified for the day's production.

### Inspection Criteria

In order to be able to visually inspect the TAB bonds, some modifications had to be made to Honeywell's Microelectronics Workmanship Standard, U-ED23036. These modifications include: rejection of devices which exhibited less than 50% of the TAB lead width on either the chip and/or the substrate bonding pads, bonds where there is no evidence of tool impression; and on the substrate, where a TAB lead tail and any adjacent metallization is closer than 0.001 inch. Acceptable rework procedures include: circular or semicircular bond imprint on TAB lead made by the wire bond capillary tool, lead bonded on remaining portion of other lead, and wirebond on top of "bump" or wirebond in place of TAB lead.

Table 10-1. Device Assignment for Qualification Tests\*

Group "B" - 13 Devices

Lot 0001: 258, 209, 277

Lot 0002: 386, 392, 401, 403, 404, 417, 421, 423, 428, 431

Group "C" - 38 Devices

Lot 0001: 201, 202, 4, 5, 6, 12, 14, 16, 18, 19, 20, 21, 25, 26,  
228, 233, 35, 39, 40, 41, 42, 45, 49, 50, 56, 57, 61, 65,  
66, 67, 70, 72, 73, 75, 76, 80, 81, 85

Group "D" - 15 Devices

Lot 0001: 286, 93, 94, 95, 99, 302, 303, 04, 05, 06, 08, 09,  
13, 14, 15

Group "D" - S/G 2

S/N: 537, 546, 547, 549, 553, 554, 558, 559, 560, 562,  
566, 568, 569, 571, 572

\*Results available in "Qualification Test Data" report at ERADCOM.

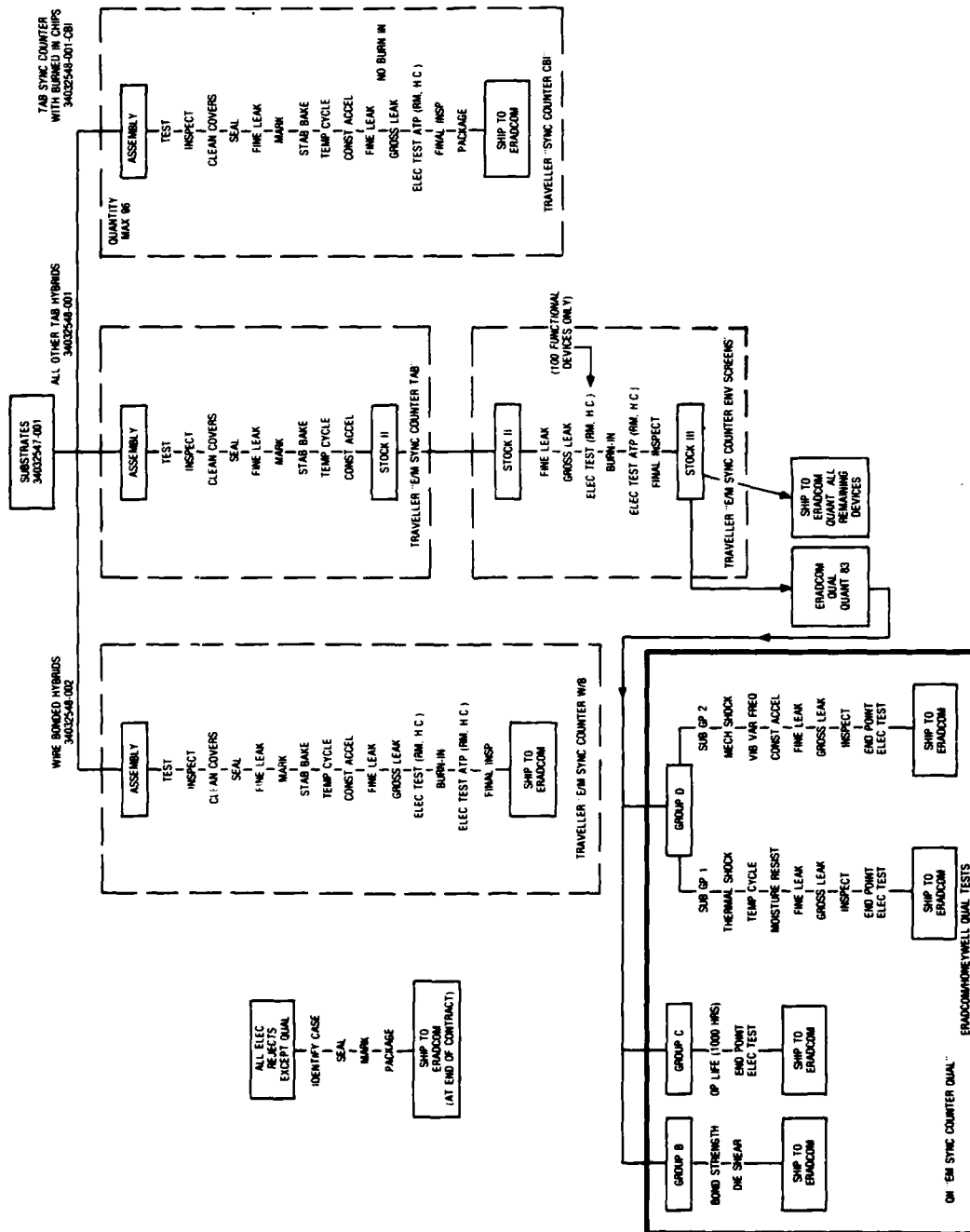


Figure 10-1. ERADCOM Qualification



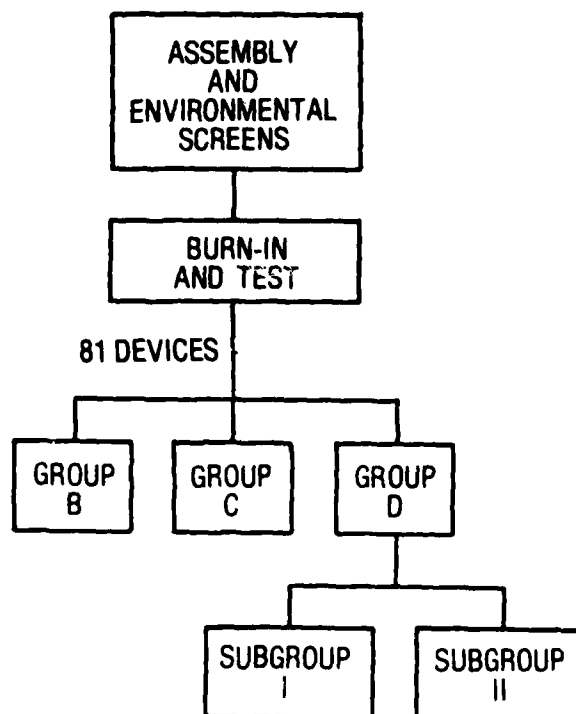


Figure 10-2. TAB Qualification Schedule

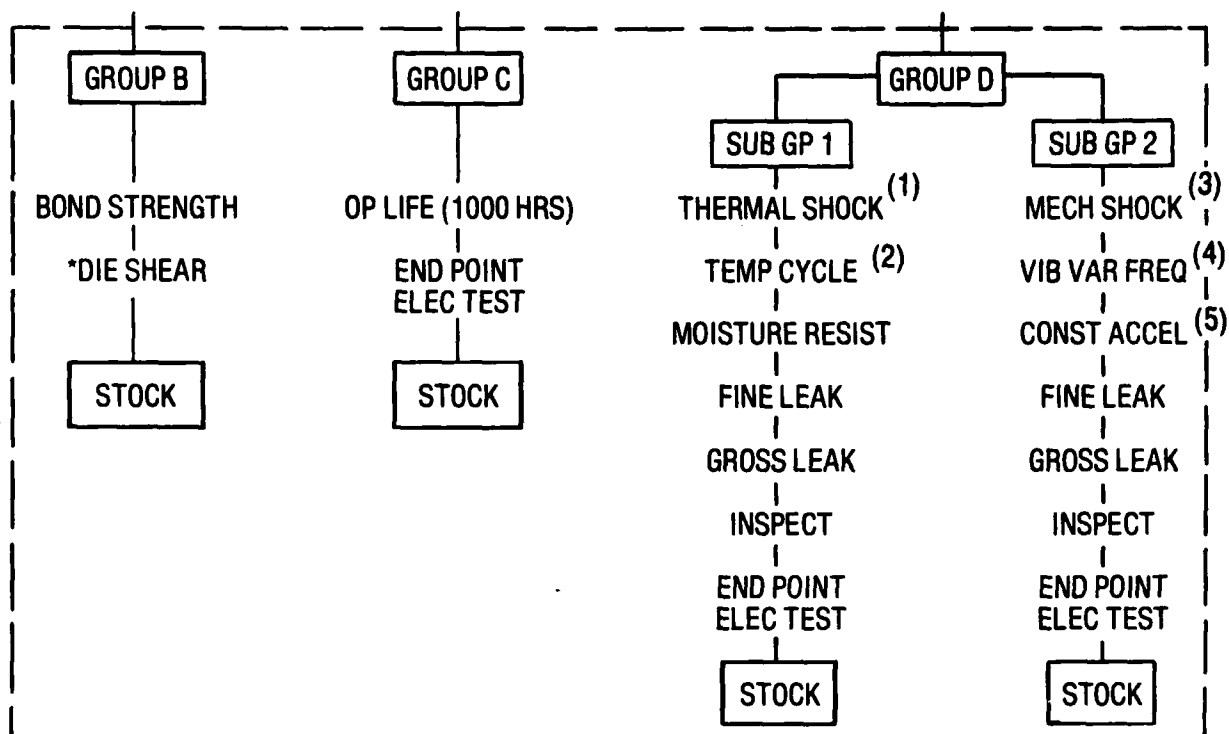


Figure 10-3. ERADCOM/Honeywell Qualification Tests

All tests in accordance with MIL-STD-883

- (1) Method 1011 Cond B 15 cycles min
- (2) Method 1010 Cond C 100 cycles min
- (3) Method 2002 Cond C (min) Y, orientation only (3000 g's peak, 0.3 msec pulse)
- (4) Method 2007 Cond A (20 g's peak)
- (5) Method 2001 Cond A (5000 g's, Y<sub>1</sub> orientation only)

## Section 11

### COSTS

Honeywell has performed analysis of the manufacturing costs associated with TAB technology. This analysis basically consists of three different items, each one of which was addressed and reviewed separately:

- a. A theoretical cost model\*, which was generated on the basis of two hypothetical standard hybrid modules, one of low and one of high complexity.
- b. Breakout of labor by task and grade employed during the build of 1604 Hybrid Sync Counter circuits, in complexity somewhat similar to standard hybrid module number 1 of the cost module.
- c. Projected production costs of Sync Counter Hybrids build with TAB in quantities of 100, 1000, 5000 and 10,000 as compared to build with chip and wire (C&W) techniques.

Each one of the above elements will be briefly discussed below.

#### A. Cost Model

The purpose of the cost model was to analyze the production costs of hardware utilizing either conventional chip and wire (C&W) technology or Tape Automated Bonding.

The models prepared to predict production costs are based on two hypothetical hybrids of different complexity. Table 11-1 shows the makeup of standard hybrid modules I and II. Of interest is the break-even quantity of hybrids with wirebonding versus hybrids built with TAB. For Standard Module Number I this quantity is approximately 900 circuits, for Standard Module Number II approximately 200 circuits. These quantities are lower than anticipated on the basis of the nonrecurring costs, and are greatly influenced by the first electrical test yield.

Figure 11-1 shows a graph depicting the comparative cost analysis of Standard Module Number 1, Figure 11-2 shows this graph for Standard Module Number 2. Appendix III at the back of this report includes the entire cost model.

\*Cost model developed under Contract DAAK40-76-C-1079.

B. Labor Employed by Task and Grade During the Build of the E/M Sync Counter

Nine labor categories were utilized in the build of the E/M Sync Counter circuit and the hours are broken out by task. Two engineering, three technician and four assembly labor grades were employed. The breakout of hours is shown in Table 11-2.

A total of 3459 hours, of which 533 for nonrecurring tasks, were expended in the fabrication of the 1604 circuits. The remaining 2920 hours of recurring labor provide an average of 1.82 hours expended on each of the 1604 circuits fabricated. The actual hours and those calculated in the Projected Production Costs (1.82 vs 1.88) correspond very closely and show the relative accuracy of the cost model.

C. Projected Production Costs

LABOR

A 1980 production quote for Sync Counters was used as the base for the C&W estimate. Hours were costed at an assembly labor grade. Material and support were held to the relative cost ratios of these items to assembly cost that occurred in the original production quote. This gives a recurring labor per unit of \$47.79, material per unit of \$34.82 and support per unit of \$100.00.

TAB hours were derived from process deltas to the original production quote. The areas of difference are component mount and wirebond plus inspection. Component mount was factored to 25 percent of the production effort based on a linear reduction of the effort based on one cap to mount versus one cap and three chips in chip and wire. Operation of chip separation; inner and out lead bonding, chip test, and framing based on the standards in the cost model using an EHR\* of 3.0. Wirebond and inspection were limited to the manually wirebonded wires remaining in the TAB build. Overall yields through first test for C&W (52 percent) and TAB (86 percent) show a 65.4 percent improvement for TAB that was used to factor down troubleshoot and rework hours. The hours per unit show a 48 percent reduction to 1.88 hours per unit. This delta was reviewed with the Program Manager for reasonability.

MATERIAL

The material deltas were based on actual TAB material for those items primarily lead frames.

\*EHR (Earned Hour Ratio) - The actual time required for performance of a task compared to a standard time derived from time and motion studies for that same task.

#### NONRECURRING

Nonrecurring costs are based on the cost model with a review through the Program Manager for continued cost reasonability. Lead frames design masks, IC test programs and fixturing and thermodes are the primary nonrecurring deltas.

Figure 11-3 shows the curves for production cost savings of the E/M Sync Counter built with TAB versus chip and wire. Note the crossover point at 776 devices.

Table 11-3 shows estimated costs for new production with TAB and C&W for the E/M Sync Counter in quantities of 100, 1000, 5000 and 10,000 devices.

Table 11-1. Standard Module Configurations  
Used in Cost Model

<u>Configuration</u>	<u>No. 1</u>	<u>No. 2</u>
Substrates	1	1
Layers	6	8
Size	1 x 1 inch	2 x 2 inches
IC Types	3	11
No. ICs	7	32
No. IC Wires	126	359
Projected Loss (C&W/TAB)	10%/2.5%	15%/2.5%
Resistor Chip Types	2	7
No. Resistor Chips	4	20
No. Resistor Wires	72	225
Capacitor Types	3	9
No. Capacitors	8	24
Modules/Burn-In Board	21	6

Table 11-2. Analysis of Labor Requirements for TAB Sync Counter Fabrication by Task and Grade

	Engineer		Technician			Assembly			
	I	II	I	II	III	I	II	III	IV
E/M Synchronous Counter Relayout	20	25	10	130	98				
Lead Frame and Bump Mask Design	20		40	118	128				
Plate Tape Mount and Dice Wafers	30	50	280	30	2	54	115	46	20
Substrate Fabrication (Thick Film)	12			76	63		1		
*ILB, OLB and Assembly Operations	50	18	280	243	155	541	48	5	
Circuit Electrical Test	50	64		26		20	212		
Chips-On-Tape, Burn-In	20	22	48	30	60				
Circuit Burn-In	10	40	40	84	25				
Total, by Labor Grade	212	219	698	737	531	615	376	51	20

\*This task includes all visual inspections, testing of chips-on-tape, package seal and leak test operations.

Note 1. Total circuits fabricated - 1604

Note 2. Tasks 1 and 2 involve nonrecurring labor; tasks 3-7 only involve recurring labor

Note 3. In all labor categories, the highest skill labor grades are represented by Roman Numeral I and lowest skill by Roman Numeral IV.

Table 11-3. Actual Cost - E/M Sync  
Counter Circuits

(Chip and Wire Versus TAB Process)

<u>Unit Quantity</u>	<u>C&amp;W Unit Cost \$</u>	<u>TAB Unit Cost \$</u>	<u>C&amp;W Total Cost K\$</u>	<u>TAB Total Cost K\$</u>	<u>TAB Savings K\$</u>
100	272.61	323.14	27.3	32.3	-5
1,000	194.21	189.93	194.2	189.9	4.3
5,000	184.41	178.09	922.1	890.5	31.5
10,000	183.51	176.61	1835.1	1766.1	69





Figure 11-1.

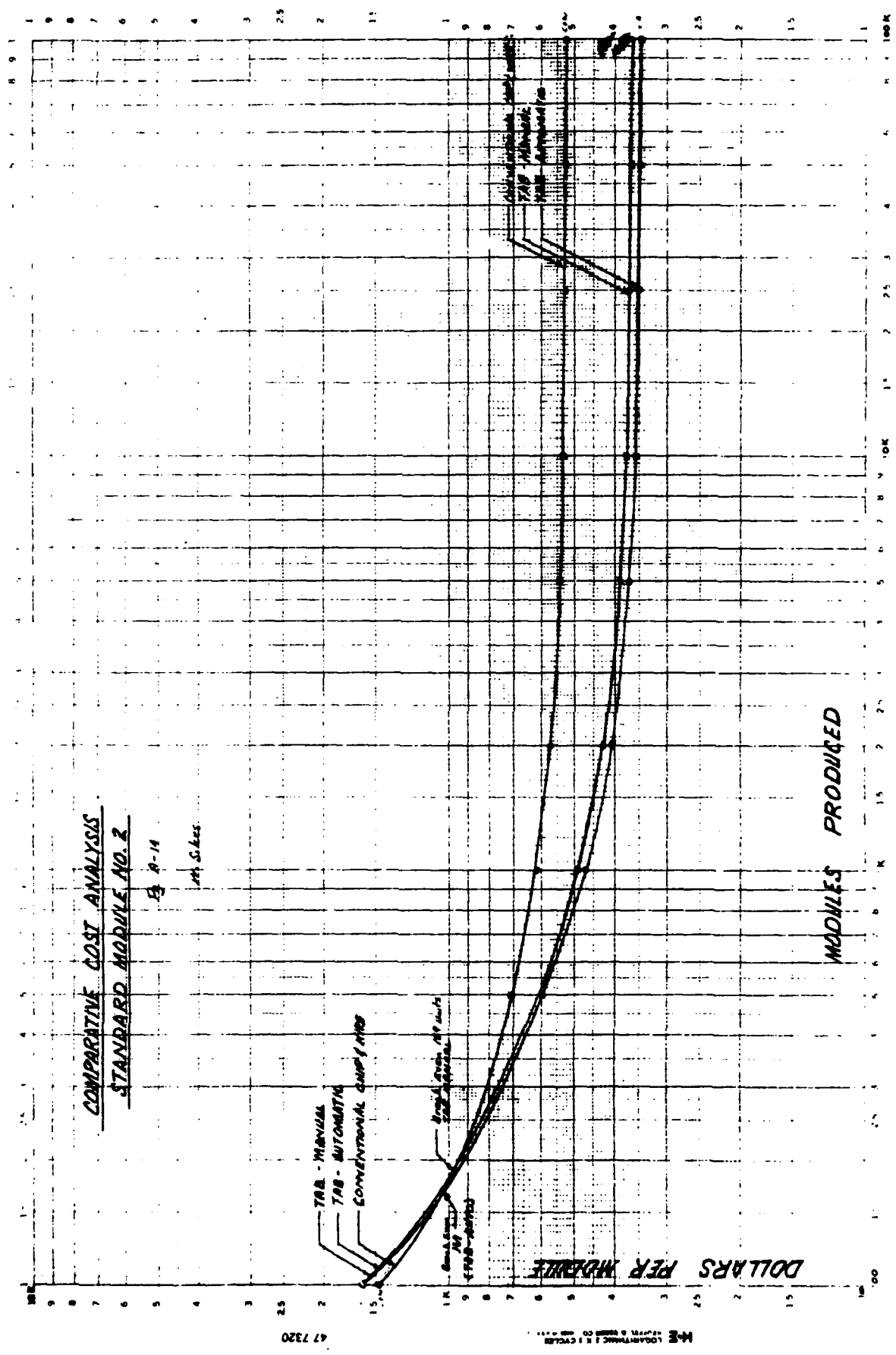


Figure 11-2.

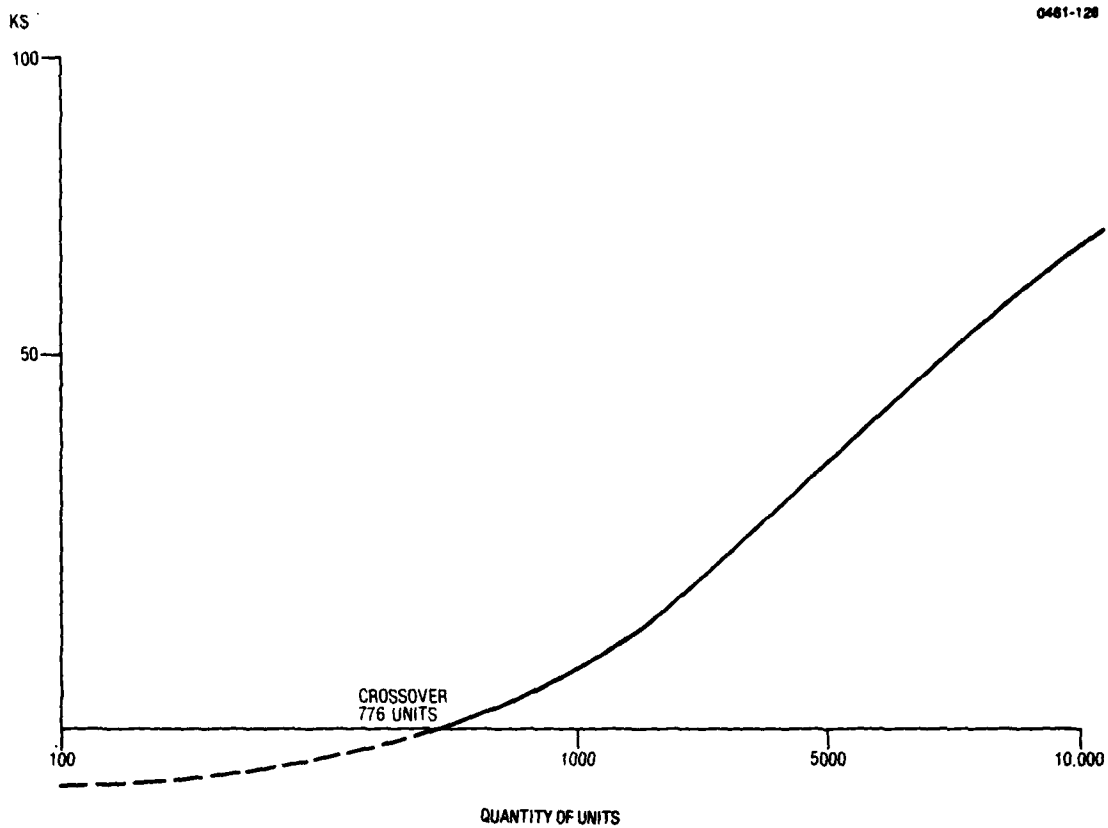


Figure 11-3. Cost Savings of TAB

## Section 12

### CONCLUSIONS

On the basis of the results of this MM&T project, Honeywell believes that TAB is a viable and successful technology. Its application will be governed by factors related to circuit design, complexity, production volume, and the final use environment.

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"Hybrids with TAB - At the Threshold of Production", William R. Rodrigues de Miranda, Proceedings of the 1979 International Microelectronics Symposium (ISHM), p. 61, November 1979.

"Tape Bonding of Large Chips", William R. Rodrigues de Miranda, NEPCON West, Anaheim, CA, February 26, 1980.

"A Review of Wafer Bumping for TAB", Dr. T.S. Liu, P.R. Zipperlin, and William R. Rodrigues de Miranda, Solid State Technology Magazine, March 1980, p. 71.

"Manufacturing of Hybrid Microcircuits with TAB", William R. Rodrigues de Miranda, Southeast Printed Circuits and Microelectronics Exposition and Conference, Orlando, FL, April 1, 1980.

"Flip-TAB Process Broadens and Improves TAB Technology", Dr. T.S. Liu, C.H. McIver and William R. Rodrigues de Miranda, 1980 ERADCOM Hybrid Microcircuit Symposium, Ft. Monmouth, NJ, June 4-6, 1980.

Appendix 1  
FAILURE ANALYSIS REPORT

ANALYTICAL SERVICES LAB  
WORK REQUESTREQUEST NUMBER - CODE  
66-F**Honeywell**

12001 STATE HIGHWAY 55, PLYMOUTH, MINNESOTA 55441, TELEPHONE 612/541-2508, 2442

PART NUMBER  
34032548PART NAME/FUNCTION  
SYNC Counter

REQUESTER	REQUESTER Will Perry		PHONE HVN 463-3856	DIVISION AvD - Florida	DEPARTMENT Hybrid
	REQUEST DATE 1/23/81	CHARGE NUMBER SD545-1000		TECHNOLOGY Hybrid/Low Power Schottky T <sup>2</sup> L	
	PART ORIGIN <input type="checkbox"/> FEASIBILITY <input type="checkbox"/> DEVELOPMENT <input type="checkbox"/> ENGINEERING <input checked="" type="checkbox"/> PROTOTYPE		ANALYSIS TYPE <input checked="" type="checkbox"/> FAILURE <input type="checkbox"/> MATERIALS <input type="checkbox"/> LINE QUALITY <input type="checkbox"/> CALIBRATION <input type="checkbox"/> OTHER		WORK REQUESTED <input checked="" type="checkbox"/> SEM-If Needed <input type="checkbox"/> EDS <input type="checkbox"/> AUGER <input type="checkbox"/> CROSS-SECTION
	<input type="checkbox"/> PRODUCTION <input type="checkbox"/> FIELD RETURN <input type="checkbox"/> OTHER		<input checked="" type="checkbox"/> ELEC. TEST <input checked="" type="checkbox"/> ELEC. PROBE <input checked="" type="checkbox"/> OPTICAL/PHOTO <input type="checkbox"/> OTHER		
	DEVICE HISTORY				
REQUESTER	<input checked="" type="checkbox"/> FAILURE		APPROXIMATE HOURS TO FAILURE 0	OPERATION ENVIRONMENT (TEMP) As Indicated	OPERATION ENVIRONMENT (HUM) N/A
	<input type="checkbox"/> OTHER				
	COMMENTS 4 failed dynamic ATP test at temp (S/N 1752 - Minus 55°C; S/N 1791, 1810 & 1818 at +100°C, all "CBI" Lot). 1 chip & wire (S/N 0110) failed 100°C test - pre B.I. 1 TAB S/N 1029 first test room temperature.				
ANALYST	WORK REQUESTED (DETAIL)  Check U <sub>2</sub> for anomalies - Devices have been delidded. Find cause of failures.				
	RESULTS (SUMMARY) S/N 1810 and 1818 were found to have contamination in the nitride. S/N 1791 exhibited contamination in a metal contact area. S/N 1029's U <sub>2</sub> chip was incorrectly bonded. S/N 1752 and 0110 contained die diffusion faults.  With exception of S/N 1029, these failures were caused by processing defects, manifested at first electrical test.				
	CORRECTIVE ACTION SHEET ATTACHED <input type="checkbox"/> YES <input checked="" type="checkbox"/> NO				
ANALYST/DATE K. Nelson c. Goelke		EST. COMP. DATE 2/14/81	DISTRIBUTION		APPROVAL Wm. Libbman 2/13/81

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ANALYTICAL SERVICES LAB  
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PROCEDURE

Optically examine for visible contamination and photograph anomalies.  
Gold coat suspect devices before SEM analysis.  
SEM photographs of anomalies.  
Etch nitride using the LFE Plasma Asher Etcher.  
Optically examine for anomalies after etch, photograph.  
Curve tracer analysis.

EQUIPMENT USED

Zeiss Universal Optical Microscope  
Denton Vacuum Sputter Coater - (Gold Coat Samples)  
SEM - Scanning Electron Microscope - JSM T-200  
LFE Plasma Asher Etcher  
Tektronix 576 Curve Tracer

ANALYSIS

Device #1810 - Contamination was observed under optical analysis (Figure 1 & 2). Device was etched in the LFE Asher Etcher to remove the nitride. After nitride was removed, the contamination present in Figure 2 was gone (Figures 3 & 4). Analysis was discontinued at this point on this device.

Device #1818 - Contamination was observed under optical examination (Figure 5 & 6). The nitride contamination is similar to that found in Device 1810. Curve tracer analysis on this device revealed no failures. This contamination could have contributed to the device failing to meet specifications at high temperature.

Device #1791 - Optical examination revealed metal contamination (Figures 7 & 8) that could, when subjected to temperature changes cause failure of the device to meet specifications. After nitride removal (Figures 9 & 19), the contamination in the metal remained. SEM analysis (Figures 11-16) indicates that this contamination is on and around the metal.

Device #1752 - Optical examination (Figures 17 & 18) revealed a processing defect possibly diffusion related. SEM analysis was performed (Figures 19-22) and indicated that the defect was below 2nd metal. The anomaly extended between to metal areas which under temperature conditions could possibly become conductive.

Device #0110 - Optical examination (Figures 23-26) indicates that there are diffusion faults present. These faults appears to occur between metal areas and below the nitride. Area indicated in Figures 24 are just two of the many possible anomalies present that could cause the failure when subjected to temperature changes.

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Device #1029 - Optical analysis (Figure 27) revealed no visible contamination that could cause a failure. Curve tracer analysis on this device indicated a short from Pin 11 to ground on Pin 16. Continued optical examination indicated the failure to be that U<sub>2</sub> (Figure 28) was bonded incorrectly.

CONCLUSION

Two devices (S/N 1810 & 1818) were found to have contamination imbedded in the nitride. One device (S/N 1791) was found to have metal contamination which under the temperature conditions may have caused the failures. Two devices (S/N 1752 and 0110) exhibited what appears to be diffusion faults in areas between metal runs. These faults could cause the devices to fail to meet specifications under the high temperature test conditions. One sample (S/N 1029) contained incorrectly bonded wires from U<sub>2</sub> to the bond pads, apparently made when replacing the tabbed chip. These wires connected the output on Pin 11 to the ground pin, and thus caused the failure.

With exception of S/N 1029, the failures were all caused due to processing defects in the chip fabrication cycle and would have been detected before assembly if the chip had seen high temperature testing prior to assembly.

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REQUEST NUMBER - CODE
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PART NUMBER
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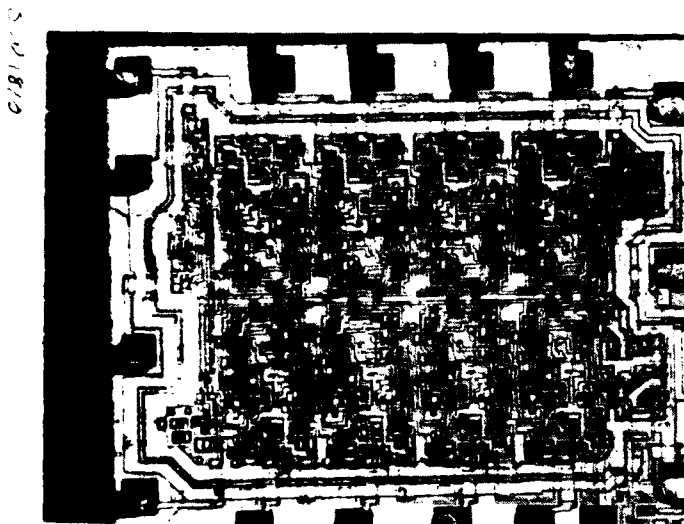


FIG 1

Figure 1. Sample 1810  
Overall view at 25X of U<sub>2</sub>.  
Curve tracer analysis on this  
device revealed no defects at  
room temp.

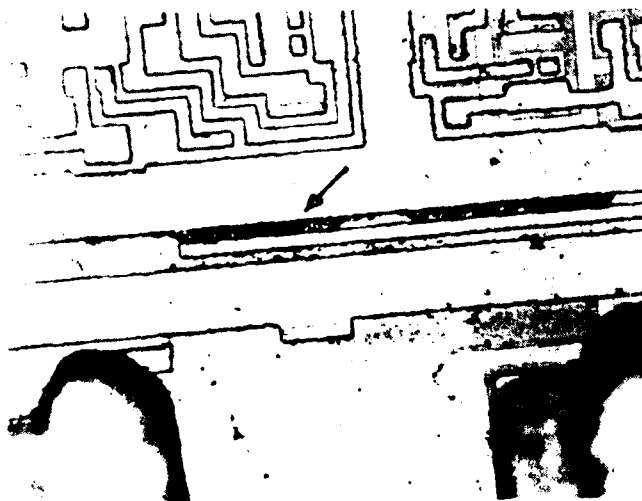


FIG 2

Figure 2. Sample 1810  
Optical photo at 261X of  
contamination.

A1-5

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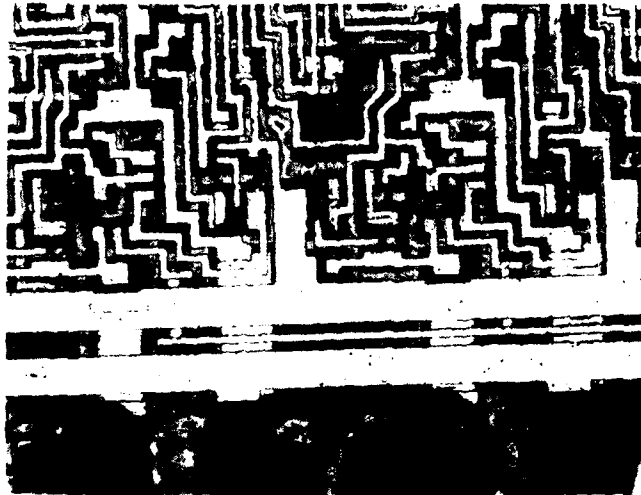


FIG 3

Figure 3. Sample 1810  
162X optical photo after  
nitride has been removed.  
Contamination that was present  
in Figure 2 is now eliminated.

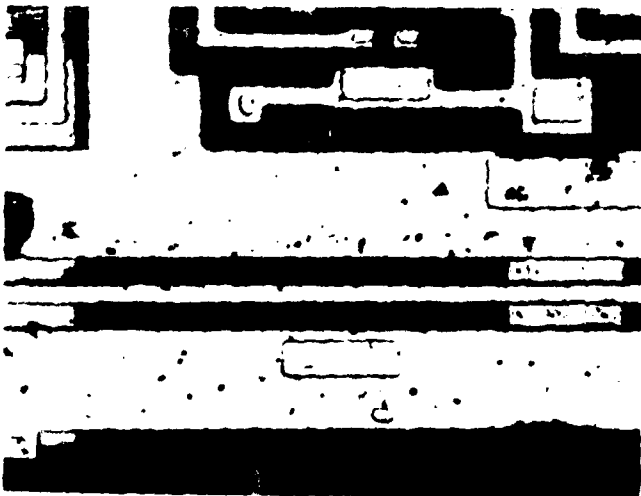


FIG 4

Figure 4. Sample 1810  
437X optical photo after  
nitride removal. Contamination  
that was present in Figure 2  
is now gone. Unable to  
determine exact cause of  
failure in this device.

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5181818

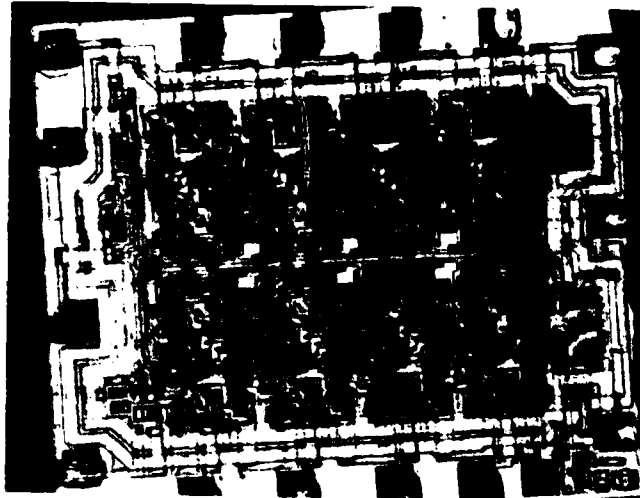


FIG 5

Figure 5. Sample 1818  
45X optical photo overall  
view of U<sub>2</sub>. Curve tracer  
analysis on this device  
indicated no failure at  
room temperature.

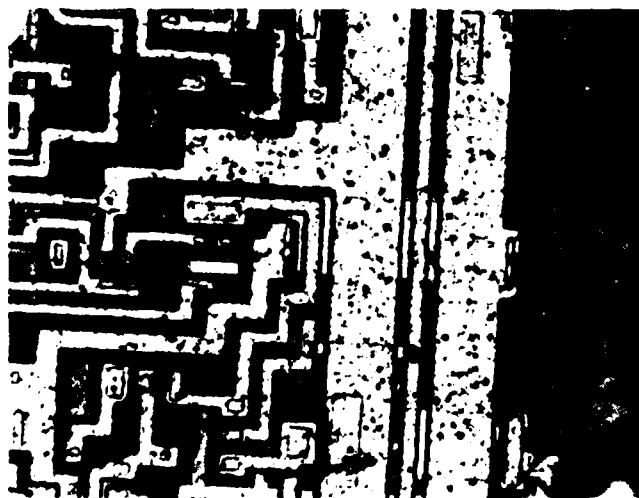


FIG 6

Figure 6. Sample 1818  
261X optical photo of con-  
tamination imbedded in the  
nitride. A similar type  
contamination is in Figure  
2, Sample 1810.

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521124

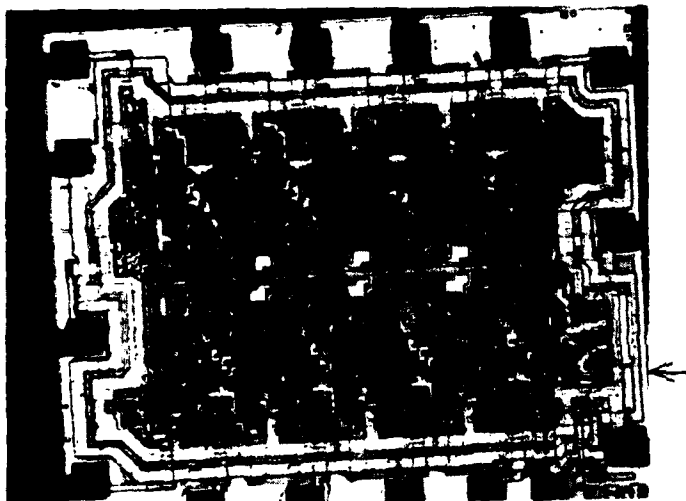


FIG 7

Figure 7. Sample 1791  
45X optical view of U<sub>2</sub>.  
Contamination site in the  
circled area.

521191

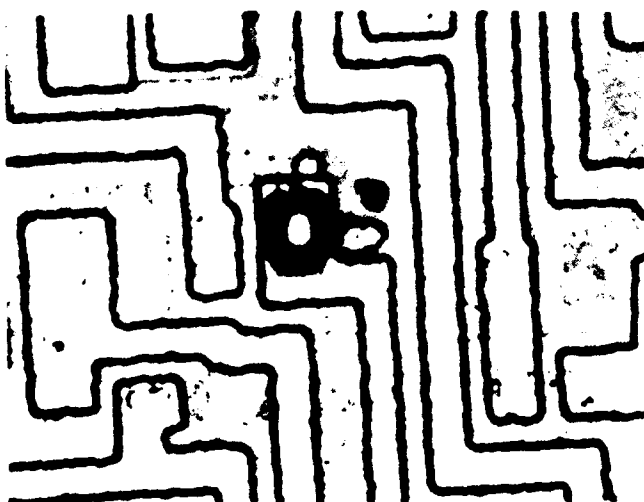


FIG 8

A1-8

Figure 8. Sample 1791  
707X optical photo of metal  
contamination in the circled  
area in Figure 7.

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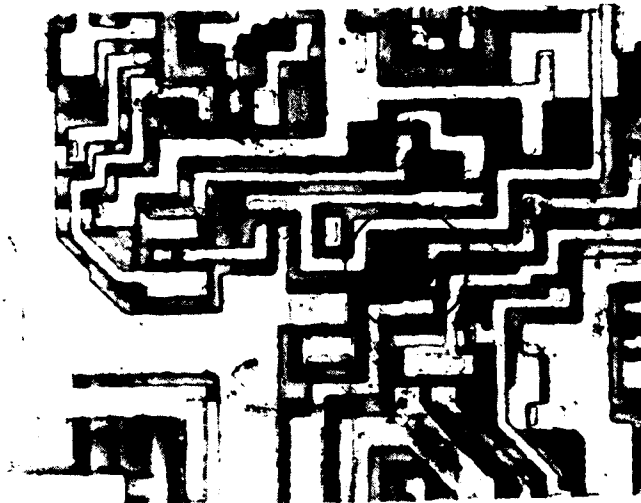


FIG 9

Figure 9. Sample 1791  
162X optical photo taken after  
asher etch of the nitride.  
Metal contamination remained.  
Same area as Figure 8.

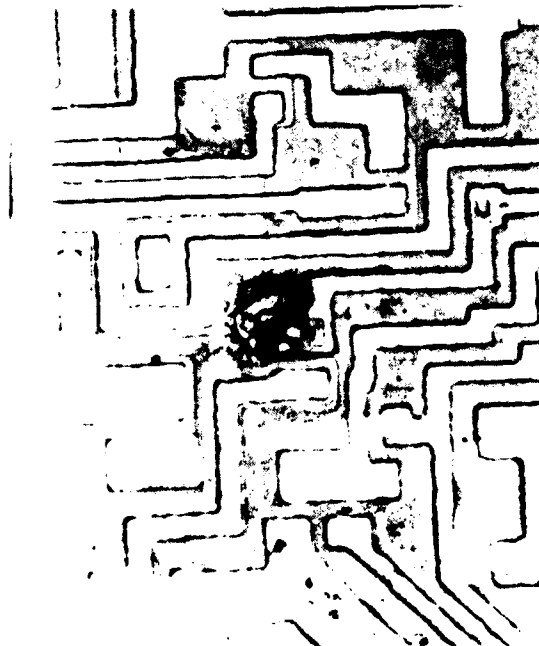


FIG 10

A1-9

Figure 10. Sample 1791  
437X optical photo taken after  
asher etch of nitride with  
metal contamination remaining.  
Same area as in Figure 8.

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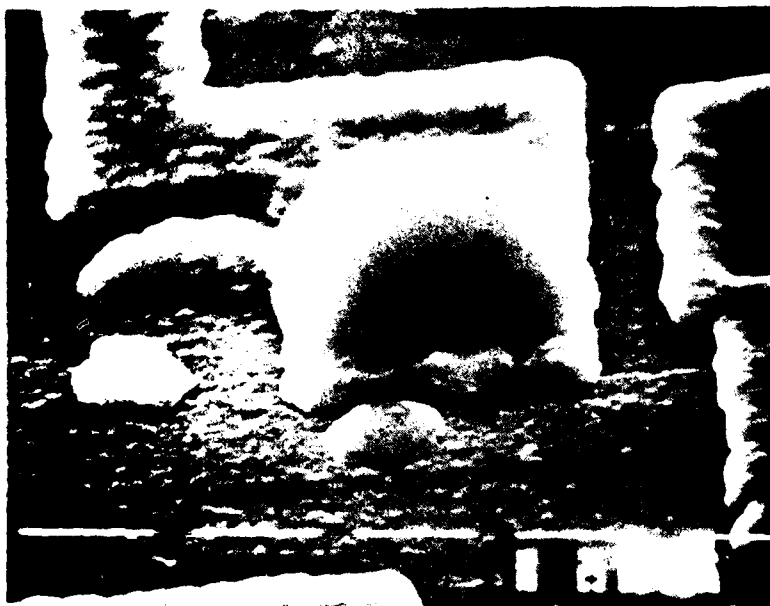


FIG 11

Figure 11. Sample 1791  
2000X 45° tilt SEM photo  
of metal contamination in  
Figure 8.

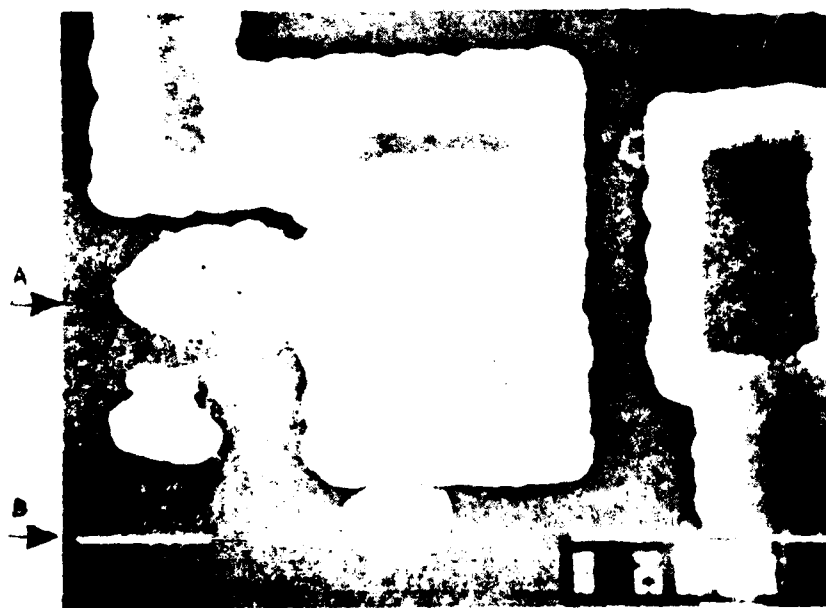


FIG 12

AI-10

Figure 12. Sample 1791  
2000X 0° tilt SEM photo  
of metal contamination.  
Same area as Figure 11.



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FIG 13

Figure 13. Sample 1791  
7500X 0° tilt close-up SEM  
photo of area A-A in Figure  
12. All SEM photos taken  
before nitride removal.

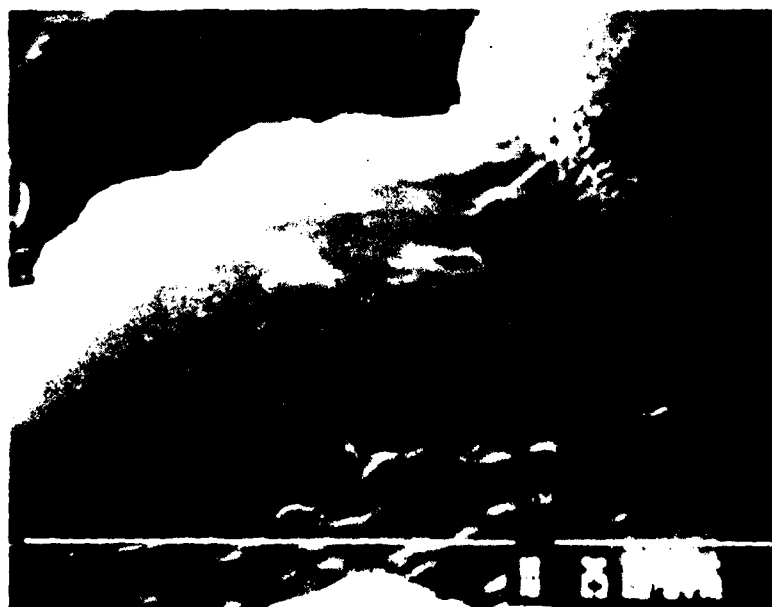


FIG 14

AI-11

Figure 14. Sample 1791  
7500X 45° tilt SEM photo  
of same area as Figure 13.

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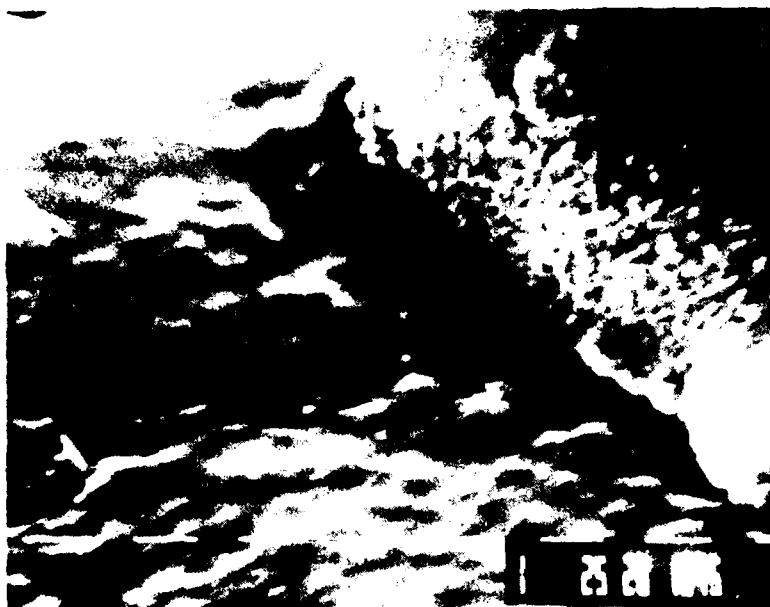


FIG 15

Figure 15. Sample 1791  
10,000X 45° tilt SEM  
photo of the area in Figure  
13.



FIG 16

Figure 16. Sample 1791  
7500X 45° tilt SEM photo  
of Area B-B in Figure 12.

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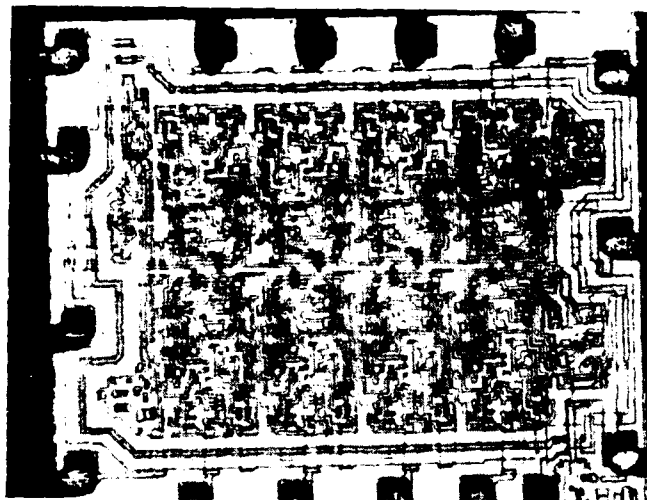


Figure 17. Sample 1752  
45X optical photo of U<sub>2</sub>.

FIG 17

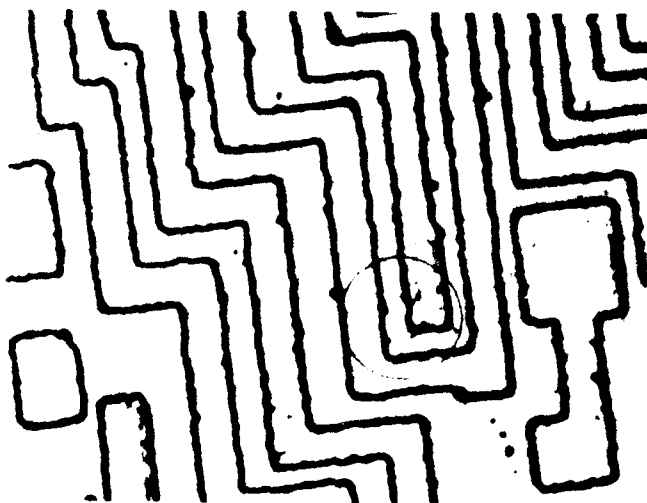


Figure 18. Sample 1752  
141X optical photo of  
possible failure causing  
processing defect.

FIG 18

A1-13

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FIG 19

Figure 19. Sample 1752  
5000X 0° tilt SEM photo  
of processing defect in  
Figure 18.



FIG 20

A1-14

Figure 20. Sample 1752  
7500X 45° tilt SEM photo  
of processing defect in  
Figure 19. Possible failure  
causing anomalie.

ANALYTICAL SERVICES LAB  
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FIG 21

Figure 21. Sample 1752  
7500X 40° tilt SEM photo  
of processing defect in  
Figure 20.



FIG 22

A1-15

Figure 22. Sample 1752  
20,000X 40° tilt SEM photo  
of processing defect in  
Figure 21.

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0110 NC

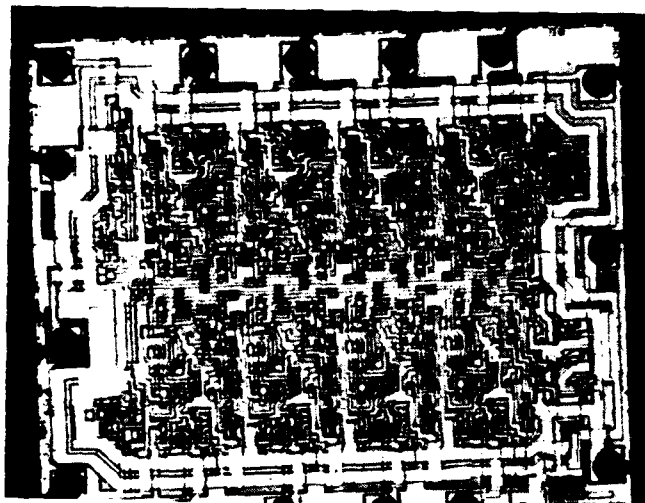
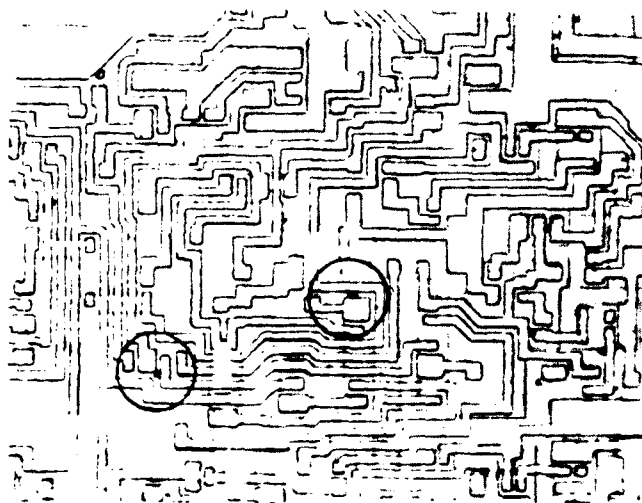


FIG 23

Figure 23. Sample 0110  
45X optical overall view  
of U<sub>2</sub>.



A

B

FIG 24

Figure 24. Sample 0110.  
162X optical photo of  
possible failure causing  
diffusion faults. Anomalies  
appear to occur below the  
oxide and nitride.

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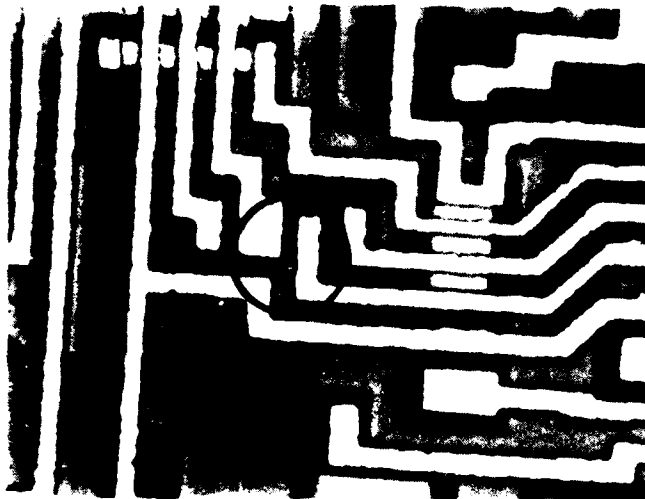


FIG 25

Figure 25. Sample 0110  
437X optical photo of  
possible failure causing  
diffusion faults. Area A  
of Figure 24.

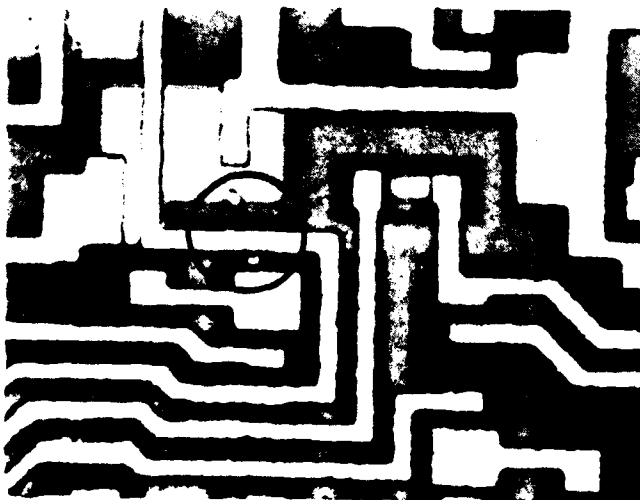


FIG 26

Figure 26. Sample 0110  
437X optical photo of  
possible failure causing  
diffusion faults. Area B  
in Figure 24.

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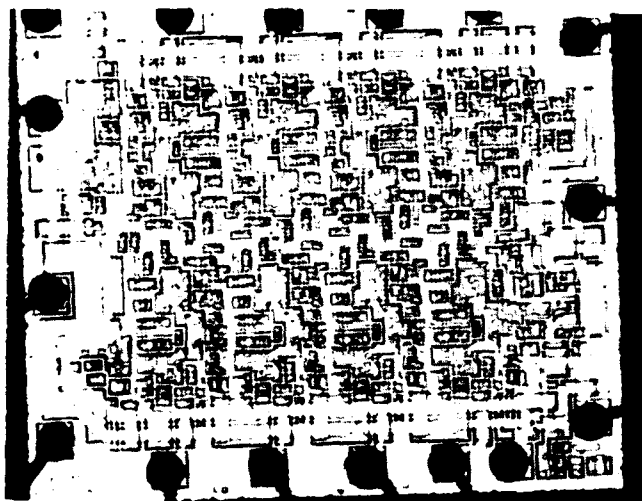
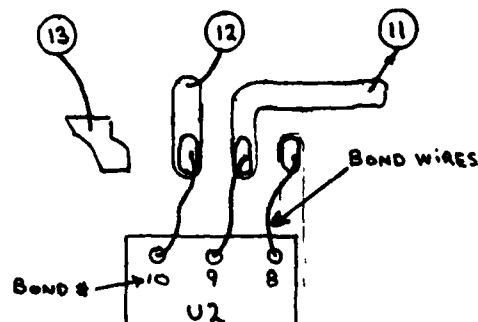


Figure 27. Sample 1029  
Overall view of 45X of U<sub>2</sub>.  
No contamination visible.



Figure 28. Sample 1029  
29X optical photo of failure mode. Three bond wires are shifted over and bonded to the wrong area. Pin 11 bond wire should be on the center bond bump in this Figure. Curve tracer analysis indicated a short to ground on Pin 11. Bond wire that is connected to Pin 13 should be on Pin 12.



A1-18



Appendix II  
ANALYSIS REPORT, NO. V02907

AD-A104 393

HONEYWELL INC CLEARWATER FL AVIONICS DIV F/6 9/5  
MANUFACTURING METHODS AND TECHNOLOGY ENGINEERING FOR TAPE CHIP --ETC(U)  
AUG 81 W R RODRIGUES DE MIRANDA, W O PERRY DAAB07-77-C-0526

UNCLASSIFIED

DELET-TR-77-0526F

NL

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DATE

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# PRODUCT ASSURANCE

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## LABORATORY

HONEYWELL  
Avionics Division  
St. Petersburg FL

### ANALYSIS REPORT

ANALYSIS NO.  
V02907

DATE ISSUED  
21 JANUARY 1981

PART NAME AND DESCRIPTION E/M SYNC. COUNTER	VENDOR NAME HONEYWELL	REQUESTER D. WRIGHT	LOT/AR/ST	
PROGRAM NAME 4843	PART NUMBER 34032548	VENDOR PART NUMBER -	DATE CODE 0423	SAMPLE 1

CONCLUSIONS:  
NO DIE/MOUNT CONTAMINATION DETECTABLE - EPOXY THIN & POROUS

#### REASON FOR ANALYSIS

TWO OF THE THREE PACKAGE DICE FAILED DIE SHEAR TEST. DETERMINE CAUSE.

#### RESULTS

A SEM/EDS ANALYSIS OF THE MATING EPOXY AND DIE SURFACES SHOWED NO DETECTABLE CONTAMINATION. THE EPOXY SURFACE UNDER THE FAILED DICE WAS FOUND TO BE MORE POROUS/VOIDED THAN UNDER THE NON-FAILURE. SEE FIGURE 1. THIS MAY HAVE PROVIDED A REDUCED BOND SURFACE AREA WHICH CONTRIBUTED TO THE FAILURE.

IT IS RECOMMENDED THAT FURTHER CONTAMINATION IDENTIFICATION TECHNIQUES BE PURSUED, PARTICULARLY IN THE ORGANIC SPECTRA.

IDB PG  
WH100 47

PREPARED BY  
W. HEUBAUM

A2-2

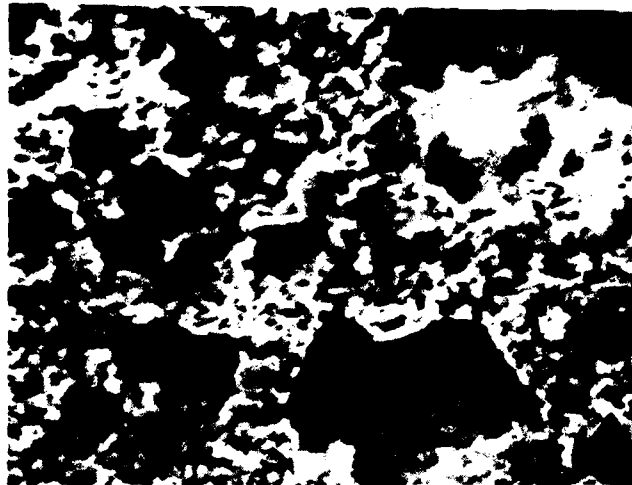
BY

DATE

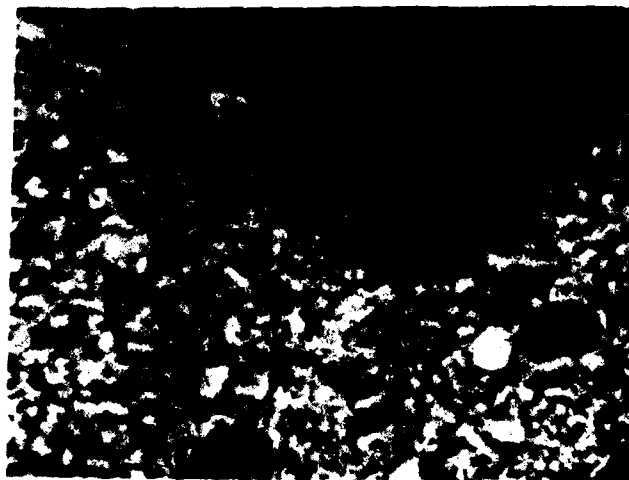
*W. Heubaum*

*J. M. Jasper*

*1-21-81*



FAILED EPOXY SURFACE (~500X)



NON-FAILED EPOXY SURFACE (~500X)

FIGURE 1  
SEM VIEWS OF EPOXY MOUNT SURFACES

A2-3

Appendix III  
COST MODEL

TAPE AUTOMATED BONDING

VS.

CONVENTIONAL CHIP & WIRE

COST MODEL

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MATERIAL COSTS	A3-11
REWORK	A3-12
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## INTRODUCTION

The following is a cost model intended for use in calculating production costs of hardware utilizing either conventional chip and wire technology or tape automated bonding. The model is organized as follows:

### Section I

This section displays 23 Recurring Process Cost Formulas which may be used in combinations to calculate the recurring assembly costs of any module. The formulas are broken into two major sections: "Conventional Processes" and "T.A.B. Processes". They are designated with the prefix letters "C" or "T", respectively. (A3-6 - A3-9)

### Section II

This section displays 9 Non-Recurring Cost Formulas which may be used in combinations to calculate the non-recurring assembly costs of any module. These formulas are designated with the prefix letters "NR". (A3-10)

### Section III

This section displays 11 Material Cost Formulas which may be used in combinations to calculate the material costs of any module. These formulas are designated with the prefix letter "M". (A3-11)

### Section IV

Page A3-12 displays the statistical relationship between individual I.C. chip yields and overall package yields varying with the number of I.C. chips per package. This information is utilized in the following Recurring Process Cost Formulas:

<u>Process No.</u>	<u>Process</u>
C-8	Troubleshoot
C-9	Rework
C-10	Re Burn-in
C-11	Re Package Test
T-7	Rework

Page A3-13 displays the relationship between I.C. chips per module and troubleshoot hours per module. This information is utilized in Recurring Process Cost Formula C-8, Troubleshoot.



## Appendix

The remaining pages contain two examples of application of the cost model.

Page A3-14 displays configuration information for two "standard modules". All of the information shown on this page is necessary for full application of the cost model.

Page A3-15 displays both the IC and Package Failure Rates associated with each of the two "standard modules". Calculations shown on this page are based on information contained in Section IV-1.

Pages A3-16 through A3-21 contain the application of the cost model to Standard Module No. 1. The model has been utilized to project costs for three methods:

1. Conventional Chip and Wire
2. T.A.B. - utilizing automatic equipment
3. T.A.B. - utilizing manual equipment

Page A3-22 displays the average cost of Standard Module No. 1 for volumes between 1 and 100K.

Page A3-23 displays the average cost information in graphical form as well as the breakeven points for the three processes.

Pages A3-24 through A3-29 display the same cost information for Standard Module No. 2.

# RECURRING LABOR COSTS - CONVENTIONAL PROCESSES

<u>PROCESS NO.</u>	<u>PROCESS</u>	<u>EQUIPMENT</u>	<u>PROCESS COST</u>
C-1	Thick Film Printing	Presco Printer/Dryer Tempress Lindberg Furn.	<ul style="list-style-type: none"> <li>o Clean Substrate .0012 hrs/substrate</li> <li>o Print, Dry, Fire .0019 hrs/print</li> <li>o Print, Dry .0014 hrs/print</li> </ul> Cost Formula: \$17.95 $[(.0012 \times \text{PDF}) + (.0014 \times \text{PD's})]$
C-2	Component Mount	Laurier Epoxy Bonder	<ul style="list-style-type: none"> <li>o Unload substrate, position new one .0023 hrs/comp. type</li> <li>o Load Chip .0039 hrs/chip</li> <li>o Cure .0008 hrs/mod. type</li> </ul> Cost Formula: \$17.95 $[(.0008 \times \text{types}) + (.0039 \times \text{chips})]$
C-3	Capacitor Mount	Laurier Epoxy Bonder	o Same as C-2 above.
C-4	Wire Bonding	K&S Automatic Bonder	<ul style="list-style-type: none"> <li>o Unload substrate, position new one .0050 hrs/substrate</li> <li>o Align reference points .0009 hrs/point</li> <li>o Initiate automatic mode .0001 hrs/component</li> <li>o Bond wire .00046 hrs/wire</li> </ul> Cost Formula: \$17.95 $[(.0050 \times \text{points}) + (.0001 \times \text{comp.}) + (.00046 \times \text{wires})]$
C-5	Visual Inspect & Rework	K&S Manual Bonder	<ul style="list-style-type: none"> <li>o Inspect for component position &amp; damage .0006 hrs/chip</li> <li>o Inspect wire bonds .0004 hrs/wire</li> <li>o Remove &amp; replace comps.               <ul style="list-style-type: none"> <li>• .20 hrs/IC x 7% replacement</li> </ul> </li> <li>o Remove &amp; replace wire               <ul style="list-style-type: none"> <li>• .0045 hrs/wire x 15%</li> </ul> </li> </ul> Cost Formula: \$17.95 $[(.0146 \times \text{chips}) + (.0011 \times \text{wires})]$

RECURRING LABOR COSTS - CONVENTIONAL PROCESSES  
(cont'd)

<u>PROCESS NO.</u>	<u>PROCESS</u>	<u>EQUIPMENT</u>	<u>PROCESS COST</u>
C-6	Burn-in	Burn-in oven	<ul style="list-style-type: none"> <li>o Load module to burn-in board .0028 hrs/module</li> <li>o Monitor burn-in .5 hrs/day x 7 days = 3.5 hrs/B.I. Board</li> <li>o Unload modules from burn-in board .0020 hrs/module</li> <li>Cost Formula: \$17.95</li> <li>((3.5 ÷ modules/board) + .0048)</li> </ul>
C-7	Package Test	Automatic Test Station	Cost Formula: \$17.95 x .02 hrs/module = \$0.36
C-8	Troubleshoot		Cost Formula: \$17.95 x T.S. hrs/pkg. x # failed packages
C-9	Rework	K&S Manual Bonder	<ul style="list-style-type: none"> <li>o Remove and replace component, wirebond .0320 hr/failed comp.</li> <li>Cost Formula: \$17.95 x .2000 x # failed Comps/module</li> </ul>
C-10	Re Burn-in	Burn-in Oven	Cost Formula: Initial B.I. cost x # failed packages.
C-11	Re Package Test	Automatic Test Station	Cost Formula: Initial test cost x # failed packages.
C-12	Seal Package	SSEC Pkg. Sealer	Cost Formula: \$17.95 x .016 hrs/pkg = \$0.29

# RECURRING LABOR COSTS - T.A.B. PROCESSES

PROCESS NO.	PROCESS	EQUIPMENT	PROCESS COST
T-1	Chip Separation	Dicing Saw	<ul style="list-style-type: none"> <li>o Clean Wafer .0830 hrs/wafer</li> <li>o Position wafer in holder .0396 hrs/wafer</li> <li>o Saw 2.0000 hrs/wafer</li> <li>o Fracture Scribe Lines .0500 hrs/wafer</li> <li>o Place IC in wafile pack .5000 hrs/wafer</li> <li>2.6726 hrs/wafer</li> </ul> <p>2.6726 ÷ 1000 IC's/wafer = .0027 hrs/IC            Cost Formula: \$17.95 x .0027 hrs/chip x # of chips/module</p>
T-2-A	Inner Lead Bonding (Automatic)	I/L Bonder 11000	<ul style="list-style-type: none"> <li>o Bond IC to lead frame .0010 hr/IC</li> <li>Cost Formula: \$17.95 x .0010 hrs/IC x # IC's/module</li> </ul>
T-2-M	Inner Lead Bonding (Manual)	I/L Bonder Mark IV	<ul style="list-style-type: none"> <li>o Bond IC to lead frame .0200 hr/IC</li> <li>Cost Formula: \$17.95 x .0200 hrs/IC x # IC's/module</li> </ul>
T-3-A	Chip Test (Automatic)	Automatic Test Station	<ul style="list-style-type: none"> <li>o Test IC in lead frame .0028 hr/IC</li> <li>Cost Formula: \$17.95 x .0028 hrs/IC x # IC/module</li> </ul>
T-3-M	Chip Test (Manual)	Manual Test Station	<ul style="list-style-type: none"> <li>o Test IC in lead frame .0083 hr/IC</li> <li>Cost Formula: \$17.95 x .0083 hrs/chip x # IC/module</li> </ul>
T-4-A	Framing (Automatic)	Automatic Framing Machine	<ul style="list-style-type: none"> <li>o Cut lead frame .0003 hr/IC</li> <li>Cost Formula: \$17.95 x .0003 hrs/IC x # IC/module</li> </ul>
T-4-M	Framing (Manual)	Manual Framing Machine	<ul style="list-style-type: none"> <li>o Cut lead frame .0028 hrs/IC</li> <li>Cost Formula: \$17.95 x .0028 hrs/IC x # IC/module</li> </ul>

RECURRING LABOR COSTS - T.A.B. PROCESSES  
(cont'd)

<u>PROCESS NO.</u>	<u>PROCESS</u>	<u>EQUIPMENT</u>	<u>PROCESS COST</u>
T-5-A	Outer Lead Bonding (Automatic)	O/L Bonder #4821	o Bond IC to substrate .0020 hrs/IC Cost Formula: \$17.95 x .0020 hrs/IC x # IC's/module
T-5-M	Outer Lead Bonding (Manual)	O/L Bonder #4810	o Bond IC to substrate .0083 hrs/IC Cost Formula: \$17.95 x .0083 hrs/IC x # IC's/module
T-6	Visual Inspect & Rework	Manual O/L Bonder	o Inspect for component position & damage .0006 hrs/IC o Inspect outer lead bonds .0003 hrs/bond o Remove & replace IC's .2000 hrs/IC x 7% replacement = .0140 hrs/IC Cost Formula: \$17.95 [(0.0146 x # IC's) + (.0003 x # O/L bonds)]
T-7	Rework	Manual O/L Bonder	o Remove and replace IC .2000 hrs/IC Cost Formula: \$17.95 x .2000 x # failed IC's/module

NON-RECURRING COSTS

<u>ITEM NUMBER</u>	<u>ITEM</u>	<u>COST FORMULA</u>
NR-1	Thick Film Screens	\$ 15.00/layer
NR-2	Program Automatic Wirebinder	\$ 0.15/wire
NR-3	Lead Frame/Mask Design (TAB only)	\$ 500.00/IC type
NR-4	Masks (2) (TAB only)	\$ 720.00/IC type
NR-5	Thermode (TAB only)	\$ 295.00/IC type
NR-6	Test Cabling (TAB only)	\$ 50.00/IC type
NR-7	I.C. Test Program (TAB only)	\$ 950.00/IC type
NR-8	I.C. Test Fixturing (TAB only)	\$ 215.00/IC type
NR-9	Package Level Testing, Programs, Fixturing	\$3,000.00/IC

MATERIAL COSTS

<u>MATERIAL NUMBER</u>	<u>MATERIAL</u>	<u>COST FORMULA</u>
M-1	Substrate 1" x 1"	\$0.50/substrate
M-2	Substrate 2" x 2"	\$0.75/substrate
M-3	Integrated Circuits	\$1.00/I.C.
M-4	Integrated Circuits with Bumps	\$1.10/I.C.
M-5	Lead Frame	\$0.70/I.C.
M-6	Resistor Chip	\$1.00/Resistor Chip
M-7	Capacitor	\$1.00/Capacitor
M-8	Gold Wire	\$0.01/Wire Bond
M-9	Thick Film Inks	\$0.90/Print
M-10	Package	\$9.75/Package
M-11	Lid	\$3.75/Lid

# PLOT OF $Y_1 = Y_p^N$

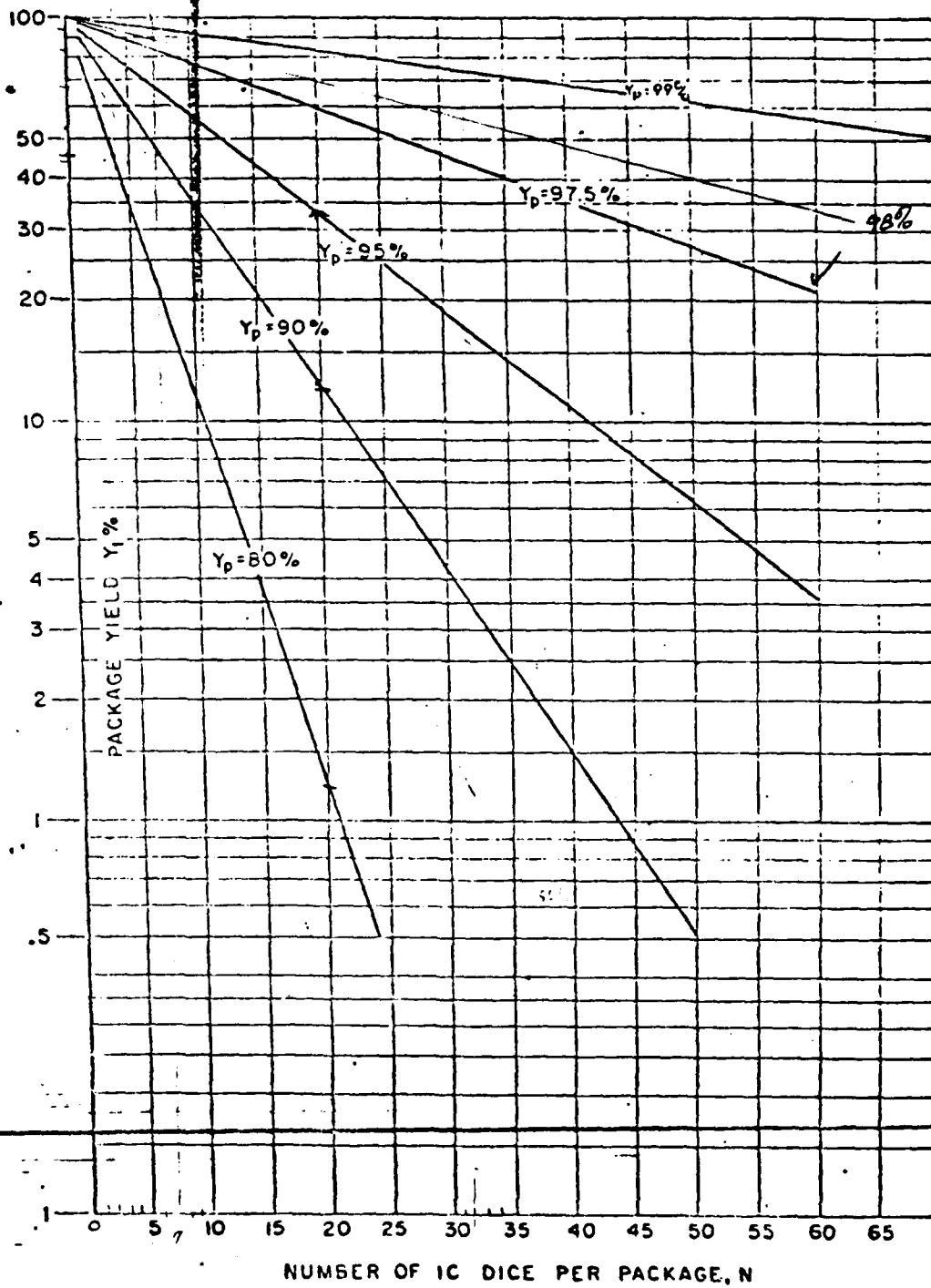
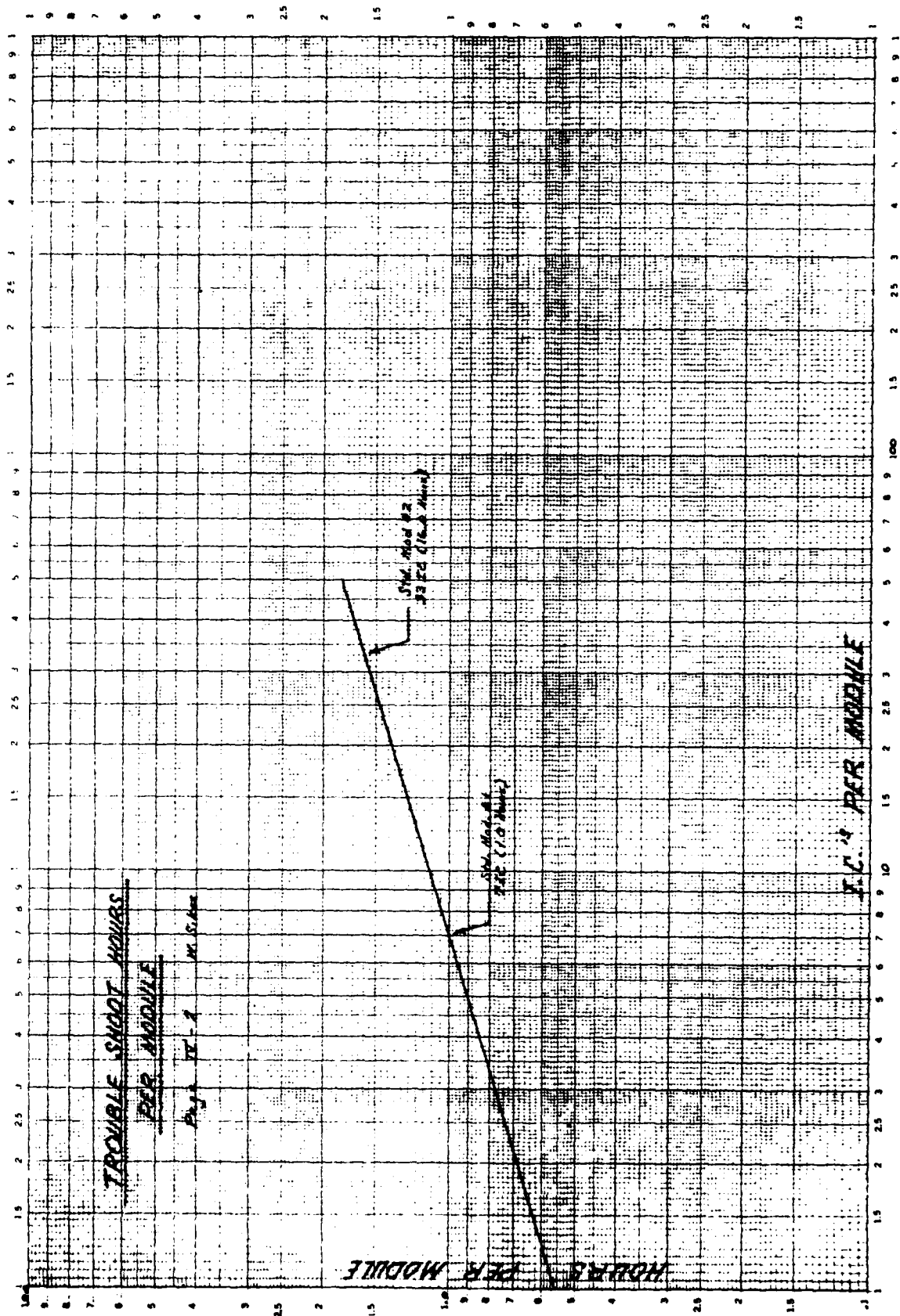


Figure 1





47 7320

A3-13

MEASUREMENTS & CYCLES  
REPRODUCED FROM 11-11-11

### STANDARD MODULE CONFIGURATION

Substrates	1	1
Layers	6	8
Size	1" x 1"	2" x 2"
I.C. Types	3	11
No. IC's	7	32
No. IC Wires	126	359
Projected Loss (C&W/TAB)	10%/2.5%	15%/2.5%
Resistor Chip Types	2	7
No. Resistor Chips	4	20
No. Resistor Wires	72	225
Capacitor Types	3	9
No. Capacitors	8	24
Modules/Burn-in Board	21	6

# PACKAGE FAILURE RATE

## CHIP & WIRE

## T.A.B.

STD. MOD. NO.	NO. IC'S/ PKG.	CHIP FAILURE RATE	TEST NO.	NO. FAILED IC'S	NO. (1) FAILED PKGS	NO. STOCKED PKGS	CHIP FAILURE RATE	TEST NO.	NO. FAILED IC'S	NO. (1) FAILED PKGS	NO. STOCKED PKGS
1	7	10% ↓	1	.700	.53	.47	2.5%	1	.175	.17	.83
			2	.070	.05	.48		2	.004	.01	.16
			3	.007	.01	.04		3	0	0	0
			4	.000	.00	.01			.18	.18	1.0
				.78	.59	1.00					
2	32	15% ↓	1	4.800	.99	.01	2.5%	1	.800	.55	.45
			2	.720	.15	.84		2	.020	.01	.54
			3	.108	.02	.13		3	.000	.00	.01
			4	.016	.01	.01			.820	.56	1.00
			5	.000	.00	.01					
				5.644	1.17	1.00					

A3-15

(1) Ref. Plot of  $Y_t = Y_p^N$

STANDARD MODULE NO. 1 - CONVENTIONAL CHIP & WIRE

RECURRING LABOR COSTS:

<u>PROCESS</u>	<u>PROCESS NUMBER</u>	<u>COST FORMULA</u>	<u>COST PER MODULE</u>
Thick Film Printing	C-1	\$17.95 $(.0012 + (.0019 \times 4) + (.0014 \times 2))$	\$ 0.21
Component Mount	C-2	\$17.95 $(.0008 + (.0023 \times 5) + (.0039 \times 11))$	0.99
Capacitor Mount	C-3	\$17.95 $(.0008 + (.0023 \times 3) + (.0039 \times 8))$	0.70
Wire Bonding	C-4	\$17.95 $(.0050 + (.0009 \times 24) + (.0001 \times 11) + (.00046 \times 198))$	2.13
Visual Inspect & Rework	C-5	\$17.95 $(.0146 \times 11) + (.0011 \times 198)$	6.79
Burn-in	C-6	\$17.95 $(3.5 \div 21) + .0048$	3.08
Package Test	C-7	\$17.95 $\times .02$	0.36
Troubleshoot	C-8	\$17.95 $\times 1.0 \times .59$	10.59
Rework	C-9	\$17.95 $\times .2000 \times .78$	2.80
Re Burn-in	C-10	\$3.08 $\times .59$	1.82
Re Package Test	C-11	\$0.36 $\times .59$	0.21
Seal Package	C-12	\$17.95 $\times .016$	0.29
TOTAL RECURRING COST =			\$29.97

NON-RECURRING COSTS:

<u>ITEM</u>	<u>ITEM NUMBER</u>	<u>COST FORMULA</u>	<u>TOTAL NON- RECURRING</u>
Thick Film Screens	NR-1	\$15.00/layer $\times 6$ layers	90.00
Program Auto Wirebinder	NR-2	\$0.15/wire $\times 198$ wires	30.00
Pkg. Level Test, Progs., Fixt.	NR-9	\$3000/IC $\times 7$ IC's	\$21,00.00
TOTAL NON-RECURRING =			\$21,120.00

STANDARD MODULE NO. 1 - CONVENTIONAL CHIP & WIRE  
(cont'd)

MATERIAL COSTS:

<u>MATERIAL</u>	<u>MATERIAL NUMBER</u>	<u>COST FORMULA</u>	<u>MATERIAL COSTS</u>
Substrate 1" x 1"	M-1	\$0.50/sub. x 1 sub./module	0.50
Integrated Circuit	M-3	\$1.00/IC x 7 IC/mod	7.00
Resistor Chip	M-6	\$1.00/chip x 4 chips/mod	4.00
Capacitor	M-7	\$1.00/cap x 8 caps/mod	8.00
Gold Wire	M-8	\$0.01/wire x 198 wires	1.98
Thick Film Inks	M-9	\$0.90/print x 6 layers	5.40
Package	M-10	\$9.75 x 1 pkg/module	9.75
Lid	M-11	\$3.75 x 1 pkg/module	3.75
			<u>\$40.38</u>

TOTAL MATERIAL COST =

# STANDARD MODULE NO. 1 - AUTOMATIC T.A.B. PROCESSES

RECURRING LABOR:		PROCESS	PROCESS	COST FORMULA	COST PER
		NUMBER	NUMBER		MODULE
Thick Film Printing		C-1		\$17.95 $(.0012 + (.0019 \times 4) + (.0014 \times 2))$	\$ 0.21
Component Mount		C-2		\$17.95 $(.0008 + (.0023 \times 2) + (.0039 \times 4))$	0.38
Capacitor Mount		C-3		\$17.95 $(.0008 + (.0023 \times 3) + (.0039 \times 8))$	0.70
Wire Bonding		C-4		\$17.95 $(.0050 + (.0009 \times 10) + (.0001 \times 4) + (.0045 \times 72))$	0.85
Chip Separation		T-1		\$17.95 $\times .0027 \times 7$	0.34
Inner Lead Bonding		T-2-A		\$17.95 $\times .0010 \times 7$	0.13
Chip Test		T-3-A		\$17.95 $\times .0028 \times 7$	0.35
Framing		T-4-A		\$17.95 $\times .0003 \times 7$	0.04
Outer Lead Bonding		T-5-A		\$17.95 $\times .0020 \times 7$	0.25
Visual Inspect &		T-6		\$17.95 $\times ((.0146 \times 7) + (.0003 \times 126))$	2.51
Rework					
Visual Inspect &		C-5		\$17.95 $\times ((.0146 \times 4) + (.0011 \times 72))$	2.47
Rework		C-6		\$17.95 $\times ((3.5 \div 21) + (.0048))$	3.08
Burn in		C-7		\$17.95 $\times .02$	0.36
Package Test		C-8		\$17.95 $\times 1.0 \times .18$	3.23
Trouble Shoot		T-7		\$17.95 $\times .2000 \times .18$	0.64
Rework		C-10		\$3.08 $\times .18$	0.55
Re Burn - In		C-11		\$0.36 $\times .18$	0.06
Re Package Test		C-12		\$17.95 $\times .016$	0.29
Seal Package					
				TOTAL RECURRING COST =	\$16.44

STANDARD MODULE NO. 1 - AUTOMATIC T.A.B. PROCESSES

( cont'd )

<u>ITEM</u>	<u>ITEM NO.</u>	<u>COST FORMULA</u>	<u>TOTAL NON RECURRING</u>
Thick Film Screens	NR-1	\$15.00/Layer x 6 Layers	\$ 90
Program Auto. Wirebinder	NR-2	\$ 0.15/wire x 72 wires	11
Lead Frame/Mask Design	NR-3	\$ 500/IC Type x 3 IC Types	1500
Masks	NR-4	\$720/IC Type x 3	2160
Thermode	NR-5	\$295 x 3	885
Test Cabling	NR-6	\$50 x 3	150
IC Test Program	NR-7	\$950 x 3	2850
IC Test Fixturing	NR-8	\$215 x 3	645
Pkg. Level Testing, Progs, Fixt.	NR-9	\$3000/IC x 7 IC	21,000
		<u>TOTAL NON-RECURRING</u>	<u>\$29,291</u>

STANDARD MODULE NO. 1 - AUTOMATIC T.A.B. PROCESSES

MATERIAL COSTS:

<u>MATERIAL</u>	<u>MATERIAL NO.</u>	<u>COST FORMULA</u>	<u>MATERIAL COSTS</u>
Substrate 1" x 1"	M-1	\$0.50/sub x 1 sub/Module	\$ 0.50
Resistor Chip	M-6	1.00/chip x 4 chips/module	4.00
Integrated Circuits with Bumps	M-4	1.10/IC x TIC/Module	7.70
lead frame	M-5	0.70/IC x TIC/Module	4.90
Capacitor	M-7	1.00/cap x 8 caps/Module	8.00
Gold Wire	M-8	0.01/wire x 72 wires/Module	.72
Thick Film Inks	M-9	0.90/Print x 6 Prints	5.40
Package	M-10	9.75/Pkg x 1 Pkg/Module	9.75
Lid	M-11	3.75/Lid x 1 Lid/Module	3.75
TOTAL MATERIAL COST			<u>\$44.72</u>



STANDARD MODULE NO. 1 - MANUAL T.A.B. PROCESSES

RECURRING LABOR:

<u>PROCESS</u>	<u>PROCESS NO.</u>	<u>COST FORMULA</u>	<u>COST PER MODULE</u>
Thick Film Printing	C-1	Reff.	\$ 0.21
Component Mount	C-2	"	0.38
Capacitor Mount	C-3	"	0.70
Wire Bonding	C-4	"	0.85
Chip Separation	T-1	"	0.34
Inner Lead Bonding	T-2-M	"	2.51
Chip Test	T-3-M	TAB .0200 x 7	1.04
Framing	T-4-M	\$17.95 x .0083 x 7	0.35
Outer Lead Bonding	T-5-M	\$17.95 x .0028 x 7	1.04
Visual Inspect & Rework	T-6	\$17.95 x .0083 x 7	2.51
Visual Inspect & Rework	C-5	Reff.	2.47
Burn-In	C-6	"	3.08
Package Test	C-7	"	0.36
Trouble Shoot	C-8	"	3.23
Rework	T-7	"	0.64
RE Burn-In	C-10	"	0.55
RE Package Test	C-11	"	0.06
Seal Package	C-12	"	0.29

TOTAL RECURRING COST = \$20.61  
TOTAL COST \$29,291

(Reff. TAB Automatic )

NON-RECURRING:

COST PER MODULE  
\$44.72

(Reff. TAB Automatic )

MATERIAL COSTS:

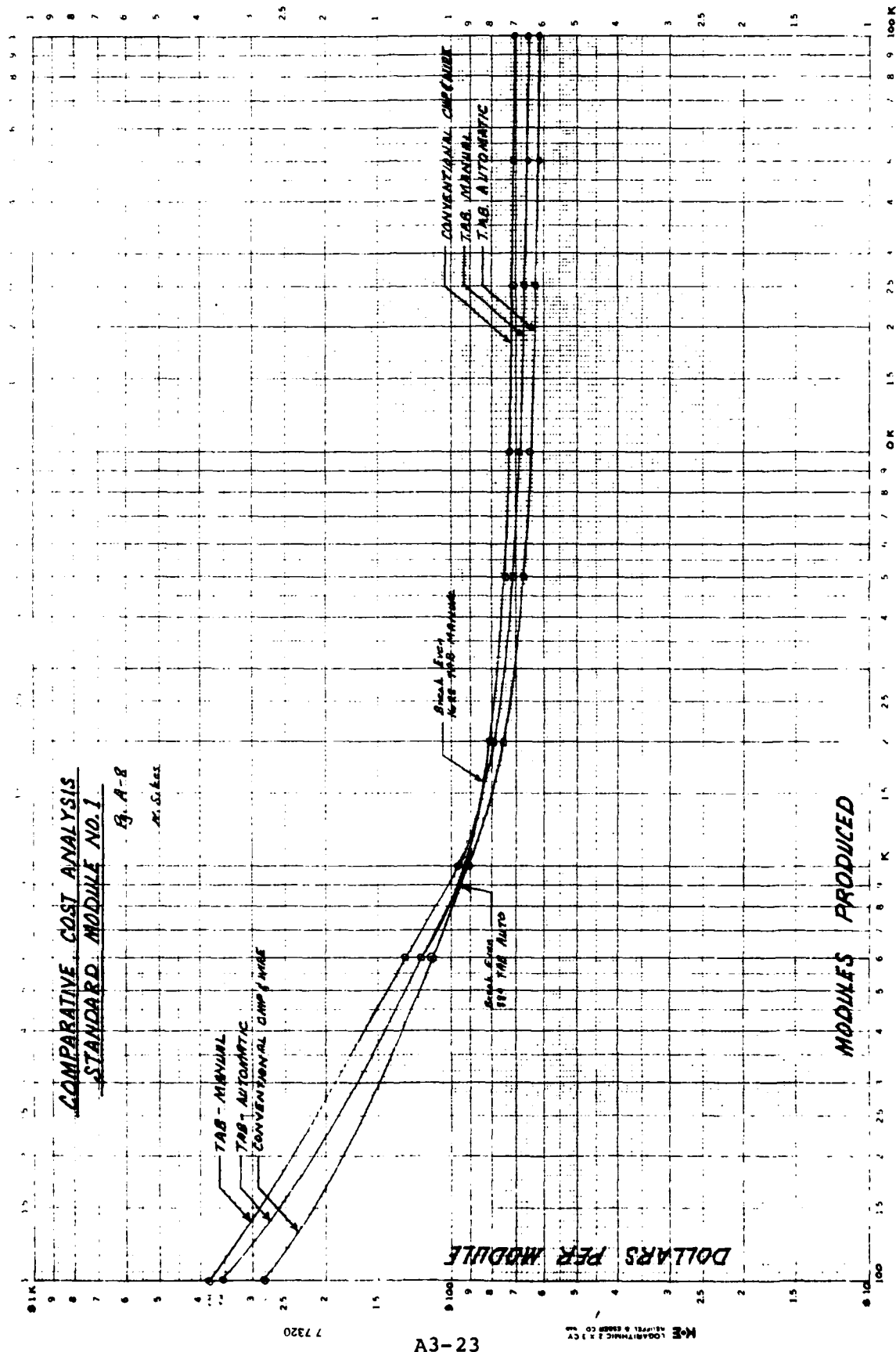
# STANDARD MODULE NO.1

CONVENTIONAL CHIP & WIRE					T. A. B. -AUTOMATIC					T. A. B. -MANUAL				
No. Units	Recur.	Non Recurr.	Mat.	Total Cost/ Module	Recur.	Non Recurring	Mat.	Total Cost/ Module	Recur.	Non Recurring	Mat.	Total Cost/ Module		
1	\$29.97	\$21,120.00	\$40.38	\$21,190	\$16.44	\$29,291.00	\$44.72	\$29,352	\$20.61	\$29,291.00	\$44.72	\$29,356		
100		211.20		281.55		292.91		354.07		292.91		328.24		
500		42.24		112.59		58.58		119.74		58.58		129.91		
1000		21.12		91.47		29.29		90.45		29.29		94.68		
2000		10.56		80.91		14.65		75.81		14.65		79.98		
5000		4.22		74.57		5.86		67.02		5.86		71.19		
10000		2.11		72.46		2.93		64.09		2.93		68.26		
25000		.84		71.19		1.17		62.33		1.17		66.50		
50000		.42		70.77		.58		61.74		.58		65.91		
100000		.21		70.56		.29		61.45		.29		65.68		

# COMPARATIVE COST ANALYSIS STANDARD MODULE NO. 1

Fig. A-8

M. S. Lee



# STANDARD MODULE NO. 2 - CONVENTIONAL CHIP & WIRE

## RECURRING LABOR COSTS:

<u>PROCESS</u>	<u>PROCESS NO.</u>	<u>COST FORMULA</u>	<u>COST/ MODULE</u>
Thick Film Printing	C-1	\$17.95 $(.0012 + (.0019 \times 5) + (.0014 \times 3))$	\$ 0.27
Component Mount	C-2	\$17.95 $(.0008 + (.0023 \times 18) + (.0039 \times 52))$	4.40
Capacitor Mount	C-3	\$17.95 $(.0008 + (.0023 \times 9) + (.0039 \times 24))$	2.07
Wire Bonding	C-4	\$17.95 $(.0050 + (.0009 \times 106) + (.001 \times 52) + (.00046 \times 584))$	6.72
Visual Inspect & Rework	C-5	\$17.95 $(.0146 \times 52) + (.0011 \times 584)$	25.16
Burn-In	C-6	\$17.95 $(3.5 \div 6) + .0048$	10.56
Package Test	C-7	\$17.95 x .02	0.36
Trouble Shoot	C-8	\$17.95 x 16.0 x 1.17	336.02
Rework	C-9	\$17.95 x .2000 x 5.644	20.26
Re Burn-In	C-10	\$10.56 x 1.17	12.36
Re Package Test	C-11	\$0.36 x 1.17	0.42
Seal Package	C-12	\$17.95 x .016	0.29

TOTAL RECURRING COST= \$418.89

## NON-RECURRING COSTS:

<u>ITEM</u>	<u>ITEM NO.</u>	<u>COST FORMULA</u>	<u>NON RECURRING</u>
Thick Film Screens	NR-1	\$15.00/Layer x 8 Layers	\$ 120
Program Auto Wirebonder	NR-2	\$0.15/Wire x 584 Wires	88
Pkg.Level Test, Progs., Fixt	NR-9	\$3000/IC x 32 IC	96,000

TOTAL NON-RECURRING \$96,208

## MATERIAL COSTS:

<u>MATERIAL</u>	<u>MAT. NO.</u>	<u>COST FORMULA</u>	<u>NON RECURRING</u>
Substrate 2" x 2"	M-2	\$0.75/sub x 1 sub/Module	\$ 0.75
Integrated Circuit	M-3	\$1.00/IC x 32 IC/Module	32.00
Resistor Chip	M-6	\$1.00/chip x 20 chips/Module	20.00
Capacitor	M-7	\$1.00/ cap x 24 caps/Module	24.00
Gold Wire	M-8	\$0.01/Wire x 584 wires/Module	5.84
Thick Film Inks	M-9	\$0.90/Print x 8 Layers/Module	7.20
Package	M-10	\$9.75 x 1 Pkg/Module	9.75
Lid	M-11	\$3.75 x 1 Pkg/Module	3.75

TOTAL MATERIAL COST \$103.29

# STANDARD MODULE NO. 2 - AUTOMATIC T.A.B. PROCESSES

## RECURRING LABOR:

<u>PROCESS</u>	<u>PROCESS NO.</u>	<u>COST FORMULA</u>	<u>COST PER MODULE</u>
Thick Film Printing	C-1	\$17.95 $(.0012 + (.0019 \times 5) + (.0014 \times 3))$	\$ 0.27
Component Mount	C-2	\$17.95 $(.0008 + (.0023 \times 7) + (.0039 \times 20))$	1.70
Capacitor Mount	C-3	\$17.95 $(.0008 + (.0023 \times 9) + (.0039 \times 24))$	2.07
Wire Bonding	C-4	\$17.95 $(.0050 + (.009 \times 42) + (.0001 \times 20) + (.00046 \times 225))$	2.66
Chip Separation	T-1	\$17.95 $\times .0027 \times 32$	1.55
Inner Lead Bonding	T-2-A	\$17.95 $\times .0010 \times 32$	.57
Chip Test	T-3-A	\$17.95 $\times .0028 \times 32$	1.61
Framing	T-4-A	\$17.95 $\times .0003 \times 32$	.17
Outer Lead Bonding	T-5-A	\$17.95 $\times .0020 \times 32$	1.15
Visual Inspect & Rework	T-6	\$17.95 $\times ((.0146 \times 32) + (.0003 \times 359))$	10.32
Visual Inspect & Rework	C-5	\$17.95 $\times ((.0146 \times 20) + (.0011 \times 225))$	9.68
Burn-In	C-6	\$17.95 $\times ((3.5 \div 6) + .0048)$	10.56
Package Test	C-7	\$17.95 $\times .02$	0.36
Trouble Shoot	C-8	\$17.95 $\times 16.0 \times .56$	160.83
Rework	T-7	\$17.95 $\times .2000 \times .82$	2.94
Re Burn-In	C-10	\$10.56 $\times 1.17$	12.36
Re Package Test	C-11	\$0.36 $\times 1.17$	0.42
Seal Package	C-12	\$17.95 $\times .016$	0.29

TOTAL RECURRING COST = \$219.51

## NON-RECURRING COSTS:

<u>ITEM</u>	<u>ITEM NO.</u>	<u>COST FORMULA</u>	<u>NON RECURRING</u>
Thick Film Screens	NR-1	\$15.00/Layer x 8 Layers	\$ 120
Program Auto Wirebonder	NR-2	\$0.15/Wire x 225 Wires	34
Lead Frame/Mask Design	NR-3	\$500/IC Type x 11 IC Types	5,500
Masks	NR-4	\$720/IC Type x 11	7,920
Thermode	NR-5	\$295 x 11	3,245
Test Cabling	NR-6	\$50 x 11	550
IC Test Program	NR-7	\$950 x 11	10,450
IC Test Fixturing	NR-8	\$215 x 11	2,365
Pkg. Level Testing, Progs, Fixt.	NR-9	\$3000/IC x 32	96,000

TOTAL NONRECURRING = \$126,184

STANDARD MODULE NO. 2 - AUTOMATIC TAB PROCESSES

<u>MATERIAL</u>	<u>MATERIAL NO.</u>	<u>COST FORMULA</u>	<u>MATERIAL COST</u>
Substrate 2" x 2"	M-2	\$0.75/sub x 1 sub/module	\$ 0.75
Integrated Circuits with Bumps	M-4	\$1.10/IC x 32 IC/module	35.20
Lead Frame	M-5	\$0.70/IC x 32 IC/module	22.40
Resistor Chip	M-6	\$1.00/chip x 20 chips/module	20.00
Capacitor	M-7	\$1.00/cap x 24 caps/module	24.00
Gold Wire	M-8	\$0.01/wire x 225 wires/module	2.25
Thick Film Ink	M-9	\$0.90/print x 8 Layers	7.20
Package	M-10	\$9.75/pkg x 1/module	9.75
Lid	M-11	\$3.75/lid x 1/module	3.75
TOTAL MATERIAL COST			\$125.30

# STANDARD MODULE NO. 2 - MANUAL T.A.B. PROCESSES

## RECURRING LABOR

<u>PROCESS</u>	<u>PROCESS NO.</u>	<u>COST FORMULA</u>			<u>COST PER MODULE</u>
Thick Film Printing	C-1	Reff.	T.A.B.	Automat.	\$ 0.27
Component Mount	C-2	"	"	"	1.70
Capacitor Mount	C-3	"	"	"	2.07
Wire Bonding	C-4	"	"	"	2.66
Chip Separation	T-1	"	"	"	1.55
Inner Lead Bonding	T-2-M	\$17.95 x	.0200 x	32	11.49
Chip Test	T-3-M	\$17.95 x	.0083 x	32	4.77
Framing	T-4-M	\$17.95 x	.0028 x	32	1.61
Outer Lead Bonding	T-5-M	\$17.95 x	.0083 x	32	4.77
Visual Inspect & Rework	T-6	Reff.	T.A.B.	Automatic	10.32
Visual Inspect & Rework	C-5	"	"	"	9.68
Burn-in	C-6	"	"	"	10.56
Pakcage Test	C-7	"	"	"	0.36
Trouble Shoot	C-8	"	"	"	160.83
Rework	T-7	"	"	"	2.94
Re Burn-in	C-10	"	"	"	12.36
Re Package Test	C-11	"	"	"	0.42
Seal Package	C-12	"	"	"	0.29

TOTAL RECURRING COST = \$238.65

NON-RECURRING:	( Reff. TAB Automatic )	TOTAL COST \$126,184.
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MATERIAL COSTS:	( Reff. TAB Automatic )	COST PER MODULE \$125.30
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STANDARD MODULE NO. 2

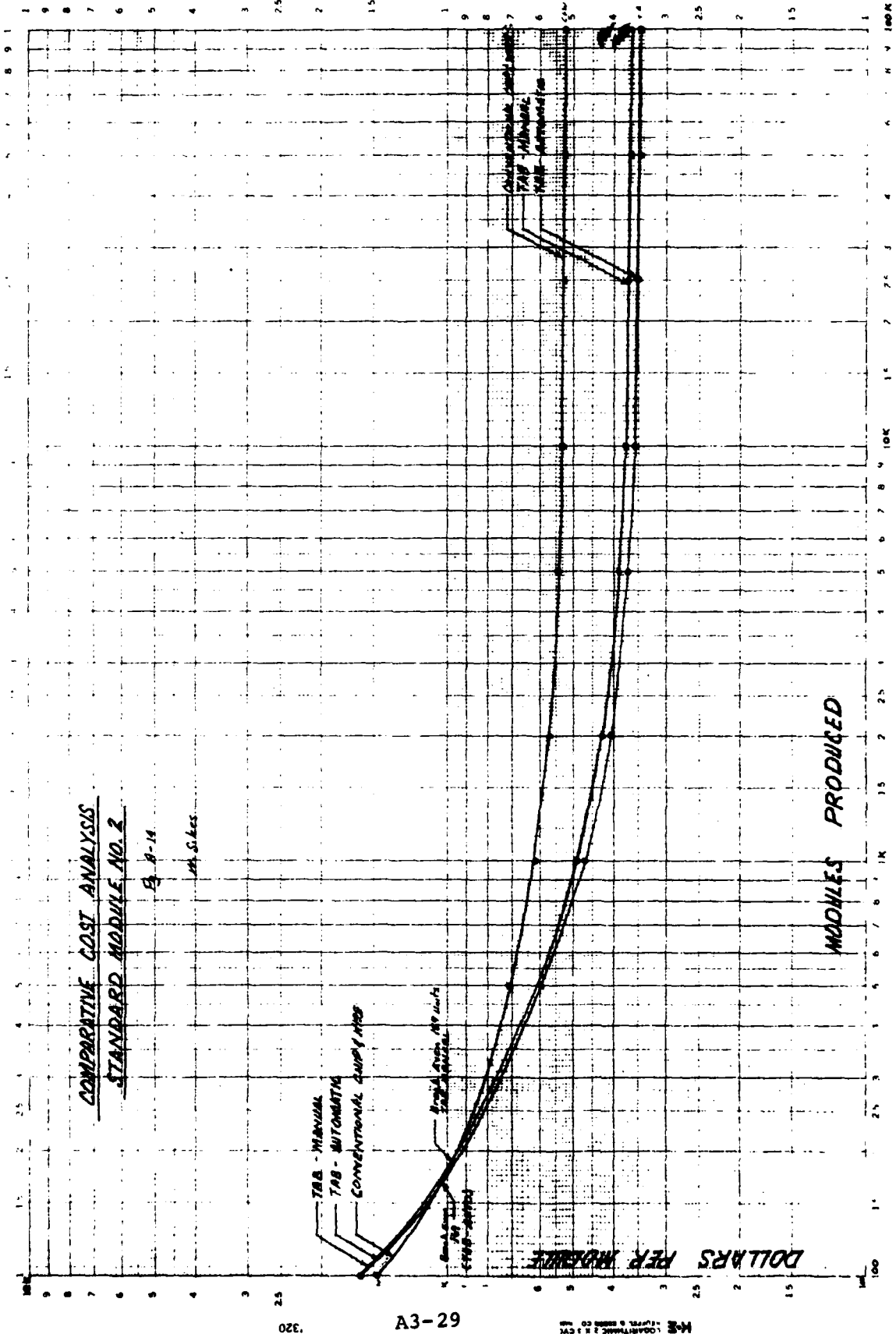
No. Units	Conventional Chip & Wire				T.A.B. - Automatic				T.A.B. - Manual			
	Recur.	Non Recur.	Mat.	Total Cost/ Module	Recurr.	Non Recurring	Mat.	Total Cost/ Module	Recurr.	Non Recurring	Mat.	Total Cost/ Module
1	\$418.89	\$96,208.	\$103.29	\$96,730	\$219.51	\$126,184.	\$125.30	\$126,529	\$238.65	\$126,184.	\$125.30	\$126,548
100		962.08		1484.26		1261.84		1606.65		1261.84		1625.79
500		192.42		714.60		252.37		597.18		252.37		616.32
1000		96.21		618.39		126.18		470.99		126.18		490.13
2000		48.10		570.28		63.09		407.90		63.09		427.04
5000		19.24		541.42		25.24		370.05		25.24		389.19
10000		9.62		531.80		12.62		357.43		12.62		376.57
25000		3.85		526.03		5.05		349.86		5.05		369.00
50000		1.92		524.10		2.52		341.33		2.52		366.47
100,000		.96		523.14		1.26		346.07		1.26		365.21



COMPARATIVE COST ANALYSIS  
STANDARD MODULE NO. 2

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